



1 pC Charge Injection, 100 pA Leakage CMOS ± 5 V/5 V/3 V 4-Channel Multiplexer

ADG604

FEATURES

- 1 pC Charge Injection (Over the Full Signal Range)
- ± 2.7 V to ± 5.5 V Dual Supply
- 2.7 V to 5.5 V Single Supply
- Automotive Temperature Range: -40°C to $+125^{\circ}\text{C}$
- 100 pA Max @ 25°C Leakage Currents
- 85 Ω Typ On Resistance
- Rail-to-Rail Operation
- Fast Switching Times
- Typical Power Consumption (<0.1 μW)
- TTL/CMOS Compatible Inputs
- 14-Lead TSSOP Package

APPLICATIONS

- Automatic Test Equipment
- Data Acquisition Systems
- Battery-Powered Instruments
- Communication Systems
- Sample and Hold Systems
- Remote-Powered Equipment
- Audio and Video Signal Routing
- Relay Replacement
- Avionics

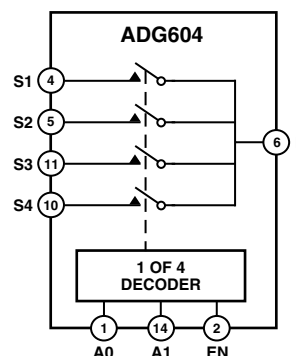
GENERAL DESCRIPTION

The ADG604 is a CMOS analog multiplexer, comprising four single channels. It operates from a dual supply of ± 2.7 V to ± 5.5 V, or from a single supply of 2.7 V to 5.5 V.

The ADG604 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. A Logic "0" on the EN pin disables the device.

The ADG604 offers ultralow charge injection of ± 1.5 pC over the entire signal range and leakage currents of 10 pA typical at 25°C . It offers on resistance of 85 Ω typ, which is matched to within 2 Ω between channels. The ADG604 also has low power dissipation yet gives high switching speeds. The ADG604 is available in a 14-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Ultralow Charge Injection (Q_{INJ} : ± 1.5 pC Typ over the Full Signal Range)
2. Leakage Current <0.5 nA max @ 85°C
3. Dual ± 2.7 V to ± 5.5 V or Single 2.7 V to 5.5 V Supply
4. Fully Specified to 125°C
5. Small 14-Lead TSSOP Package

REV. 0

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ADG604—SPECIFICATIONS

DUAL SUPPLY¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+125^{\circ}\text{C}$ unless otherwise noted.)

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V _{SS} to V _{DD}	V	V _{DD} = +4.5 V, V _{SS} = −4.5 V
On Resistance (R _{ON})	85 115	140	160	Ω Typ Ω Max	V _S = ± 3 V, I _S = −1 mA, Test Circuit 1
On Resistance Match Between Channels (ΔR _{ON})	2 4	5.5	6.5	Ω Typ Ω Max	V _S = ± 3 V, I _S = −1 mA
On-Resistance Flatness (R _{FLAT(ON)})	25 40	55	60	Ω Typ Ω Max	V _S = ± 3 V, I _S = −1 mA
LEAKAGE CURRENTS					
Source OFF Leakage I _S (OFF)	±0.01 ±0.1	±0.25	±4	nA Typ nA Max	V _{DD} = +5.5 V, V _{SS} = −5.5 V V _S = ±4.5 V, V _D = ∓4.5 V, Test Circuit 2
Drain OFF Leakage I _D (OFF)	±0.01 ±0.1	±0.5	±8	nA Typ nA Max	V _S = ±4.5 V, V _D = ∓4.5 V, Test Circuit 2
Channel ON Leakage I _D , I _S (ON)	±0.01 ±0.1	±0.5	±10	nA Typ nA Max	V _S = V _D = ±4.5 V, Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.4	V Min	V _{IN} = V _{INL} or V _{INH}
Input Low Voltage, V _{INL}			0.8	V Max	
Input Current I _{INL} or I _{INH}	0.005		±0.1	μA Typ μA Max	
C _{IN} , Digital Input Capacitance	2			pF Typ	
DYNAMIC CHARACTERISTICS ²					
Transition Time	70 100	120	150	ns Typ ns Max	V _{S1} = +3 V, V _{S4} = −3 V, R _L = 300 Ω, C _L = 35 pF, Test Circuit 4
t _{ON} Enable	80 105	130	150	ns Typ ns Max	R _L = 300 Ω, C _L = 35 pF V _S = 3 V, Test Circuit 6
t _{OFF} Enable	30 45	55	65	ns Typ ns Max	R _L = 300 Ω, C _L = 35 pF V _S = 3 V, Test Circuit 6
Break-Before-Make Time Delay, t _{BBM}	20		10	ns Typ ns Min	R _L = 300 Ω, C _L = 35 pF, V _{S1} = V _{S2} = 3 V, Test Circuit 5
Charge Injection	−1			pC Typ	V _S = 0 V, R _S = 0 Ω, C _L = 1nF, Test Circuit 7
Off Isolation	−75			dB Typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz, Test Circuit 8
Channel-to-Channel Crosstalk	−70			dB Typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz, Test Circuit 10
Bandwidth −3 dB	280			MHz Typ	R _L = 50 Ω, C _L = 5 pF, Test Circuit 9
C _S (OFF)	5			pF Typ	f = 1 MHz
C _D (OFF)	17			pF Typ	f = 1 MHz
C _D , C _S (ON)	18			pF Typ	f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	0.001		1.0	μA Typ μA Max	V _{DD} = +5.5 V, V _{SS} = −5.5 V Digital Inputs = 0 V or 5.5 V
I _{SS}	0.001		1.0	μA Typ μA Max	Digital Inputs = 0 V or 5.5 V

NOTES

¹Y Version Temperature Range: -40°C to $+125^{\circ}\text{C}$

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY¹ ($V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$. All specifications -40°C to $+125^{\circ}\text{C}$ unless otherwise noted.)

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V _{DD}	V	
On Resistance (R _{ON})	210			Ω Typ	V _{DD} = 4.5 V, V _{SS} = 0 V
	290	350	380	Ω Max	V _S = 3.5 V, I _S = −1 mA, Test Circuit 1
On Resistance Match Between Channels (ΔR _{ON})	3			Ω Typ	
		12	13	Ω Max	V _S = 3.5 V, I _S = −1 mA
LEAKAGE CURRENTS					
Source OFF Leakage I _S (OFF)	±0.01			nA Typ	V _{DD} = 5.5 V
	±0.1	±0.25	±4	nA Max	V _S = 1 V/4.5 V, V _D = 4.5 V/1 V, Test Circuit 2
Drain OFF Leakage I _D (OFF)	±0.01			nA Typ	V _S = 1 V/4.5 V, V _D = 4.5 V/1 V,
	±0.1	±0.5	±8	nA Max	Test Circuit 2
Channel ON Leakage I _D , I _S (ON)	±0.01			nA Typ	V _S = V _D = 4.5 V/1 V,
	±0.1	±0.5	10	nA Max	Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.4	V Min	
Input Low Voltage, V _{INL}			0.8	V Max	
Input Current I _{INL} or I _{INH}	0.005			μA Typ	V _{IN} = V _{INL} or V _{INH}
			±0.1	μA Max	
C _{IN} , Digital Input Capacitance	2			pF Typ	
DYNAMIC CHARACTERISTICS ²					
Transition Time	90			ns Typ	V _{S1} = 3 V, V _{S4} = 0 V, R _L = 300 Ω,
	150	185	210	ns Max	C _L = 35 pF, Test Circuit 4
t _{ON} Enable	105			ns Typ	R _L = 300 Ω, C _L = 35 pF
	150	190	220	ns Max	V _S = 3 V, Test Circuit 6
t _{OFF} Enable	45			ns Typ	R _L = 300 Ω, C _L = 35 pF
	70	80	90	ns Max	V _S = 3 V, Test Circuit 6
Break-Before-Make Time Delay, t _{BBM}	30			ns Typ	R _L = 300 Ω, C _L = 35 pF,
			10	ns Min	V _{S1} = V _{S2} = 3 V, Test Circuit 5
Charge Injection	0.3			pC Typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF, Test Circuit 7
Off Isolation	−65			dB Typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz, Test Circuit 8
Channel-to-Channel Crosstalk	−70			dB Typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz, Test Circuit 10
Bandwidth −3 dB	250			MHz Typ	R _L = 50 Ω, C _L = 5 pF, Test Circuit 9
C _S (OFF)	5			pF Typ	f = 1 MHz
C _D (OFF)	17			pF Typ	f = 1 MHz
C _D , C _S (ON)	18			pF Typ	f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	0.001			μA Typ	V _{DD} = 5.5 V
			1.0	μA Max	Digital Inputs = 0 V or 5.5 V

NOTES

¹Y Version Temperature Range: -40°C to $+125^{\circ}\text{C}$ ²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG604—SPECIFICATIONS

SINGLE SUPPLY¹

($V_{DD} = 3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$. All specifications -40°C to $+125^{\circ}\text{C}$ unless otherwise noted.)

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	$V_{DD} = 2.7\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance (R_{ON})	380	420	460	Ω Typ	$V_S = 1.5\text{ V}$, $I_S = -1\text{ mA}$, Test Circuit 1
On Resistance Match Between Channels (ΔR_{ON})			5	Ω Typ	$V_S = 1.5\text{ V}$, $I_S = -1\text{ mA}$
LEAKAGE CURRENTS					$V_{DD} = 3.3\text{ V}$
Source OFF Leakage I_S (OFF)	± 0.01 ± 0.1	± 0.25	± 4	nA Typ nA Max	$V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$, Test Circuit 2
Drain OFF Leakage I_D (OFF)	± 0.01 ± 0.1	± 0.5	± 8	nA Typ nA Max	$V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$, Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.01 ± 0.1	± 0.5	± 10	nA Typ nA Max	$V_S = V_D = 1\text{ V}/3\text{ V}$, Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V Min	
Input Low Voltage, V_{INL}			0.8	V Max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA Typ μA Max	$V_{IN} = V_{INL}$ or V_{INH}
C_{IN} , Digital Input Capacitance	2			pF Typ	
DYNAMIC CHARACTERISTICS²					
Transition Time	170 320		450	ns Typ ns Max	$V_{S1} = 2\text{ V}$, $V_{S4} = 0\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 4
t_{ON} Enable	180 250	390	450	ns Typ ns Max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$, Test Circuit 6
t_{OFF} Enable	100 160	265	390	ns Typ ns Max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$, Test Circuit 6
Break-Before-Make Time Delay, t_{BBM}	100	205	225	ns Typ ns Min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 2\text{ V}$, Test Circuit 5
Charge Injection	0.3		10	pC Typ	$V_S = 0\text{ V}$ to 3.3 V , $R_S = 0\ \Omega$, $C_L = 1\ \mu\text{F}$, Test Circuit 7
Off Isolation	-65			dB Typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 8
Channel-to-Channel Crosstalk	70			dB Typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 10
Bandwidth -3 dB	250			MHz Typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	5			pF Typ	$f = 1\text{ MHz}$
C_D (OFF)	17			pF Typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	18			pF Typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					$V_{DD} = 3.3\text{ V}$
I_{DD}	0.001		1.0	μA Typ μA Max	Digital Inputs = 0 V or 3.3 V

NOTES

¹Y Version Temperature Range: -40°C to $+125^{\circ}\text{C}$

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C unless otherwise noted)

V _{DD} to V _{SS}	13 V
V _{DD} to GND	−0.3 V to +6.5 V
V _{SS} to GND	+0.3 V to −6.5 V
Analog Inputs ²	V _{SS} −0.3 V to V _{DD} + 0.3 V
Digital Inputs ²	−0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	20 mA
Continuous Current, S or D	10 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Junction Temperature	150°C
TSSOP Package	
θ _{JA} Thermal Impedance	150°C/W
θ _{JC} Thermal Impedance	27°C/W
Lead Temperature, Soldering (10 seconds)	300°C
IR Reflow, Peak Temperature	220°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at EN, A0, A1, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model Option	Temperature Range	Package Description	Package
ADG604YRU	−40°C to +125°C	Thin Shrink Small Outline (TSSOP)	RU-14

PIN CONFIGURATION

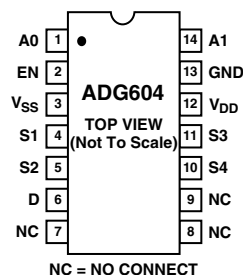


Table I. Truth Table

A1	A0	EN	ON Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

CAUTION

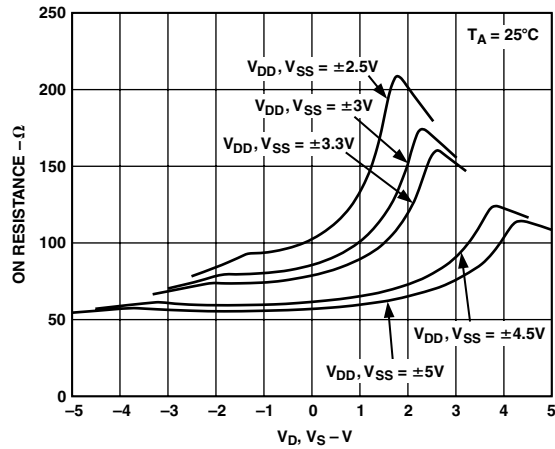
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG604 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



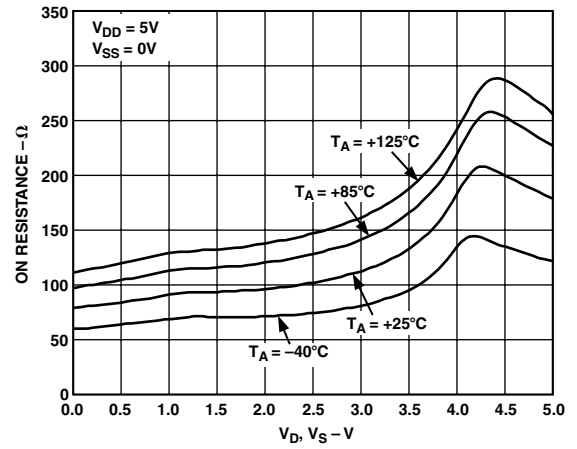
TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential
V_{SS}	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground at the device.
GND	Ground (0 V) Reference
I_{DD}	Positive Supply Current
I_{SS}	Negative Supply Current
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
R_{ON}	Ohmic Resistance between D and S
ΔR_{ON}	On Resistance Match between any two channels, i.e., $R_{ON} \text{ Max} - R_{ON} \text{ Min}$
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of On resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch “OFF”
I_D (OFF)	Drain Leakage Current with the Switch “OFF”
I_D, I_S (ON)	Channel Leakage Current with the Switch “ON”
V_D, V_S	Analog Voltage on Terminals D, S
V_{INL}	Maximum Input Voltage for Logic “0”
V_{INH}	Minimum Input Voltage for Logic “1”
$I_{INL} (I_{INH})$	Input Current of the Digital Input
C_S (OFF)	Channel Input Capacitance for “OFF” Condition
C_D (OFF)	Channel Output Capacitance for “OFF” Condition
C_D, C_S (ON)	“On” Switch Capacitance
C_{IN}	Digital Input Capacitance
$t_{ON} (EN)$	Delay time between the 50% and 90% points of the digital input and switch “ON” condition.
$t_{OFF} (EN)$	Delay time between the 50% and 90% points of the digital input and switch “OFF” condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital input and switch “ON” condition when switching from one address state to another.
t_{BBM}	“OFF” time or “ON” time measured between the 80% points of both switches, when switching from one address state to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an “On” switch.
Bandwidth	Frequency Response of the “On” Switch
Insertion Loss	Loss Due to the On Resistance of the Switch

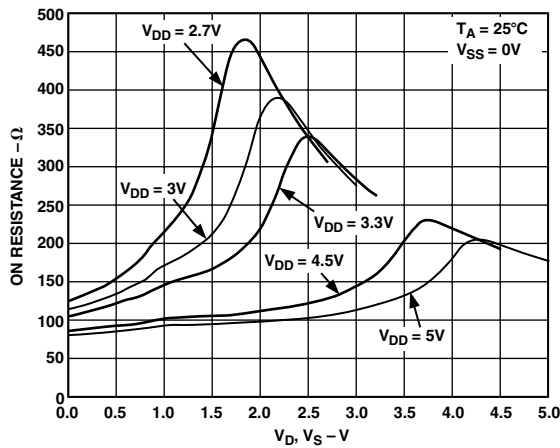
Typical Performance Characteristics—ADG604



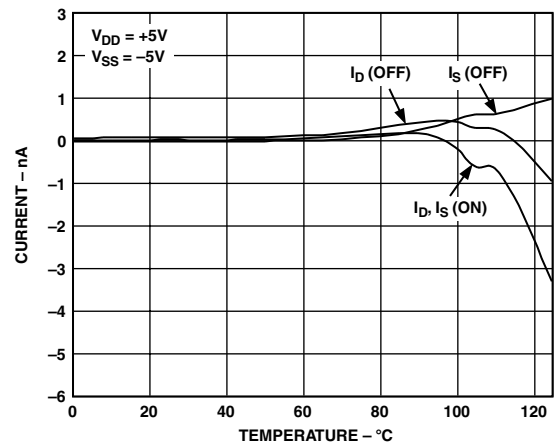
TPC 1. On Resistance vs. V_D (V_S), Dual Supply



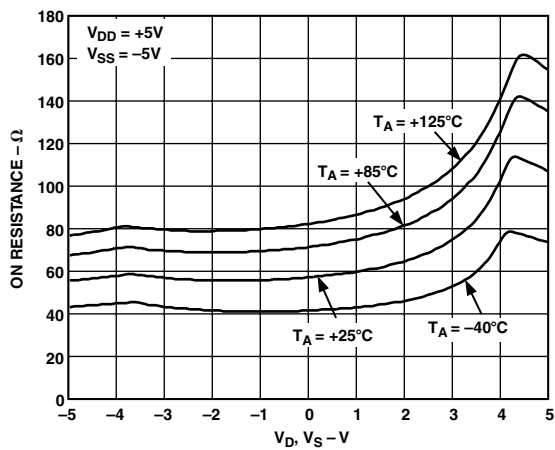
TPC 4. On Resistance vs. V_D (V_S) for Different Temperatures, Single Supply



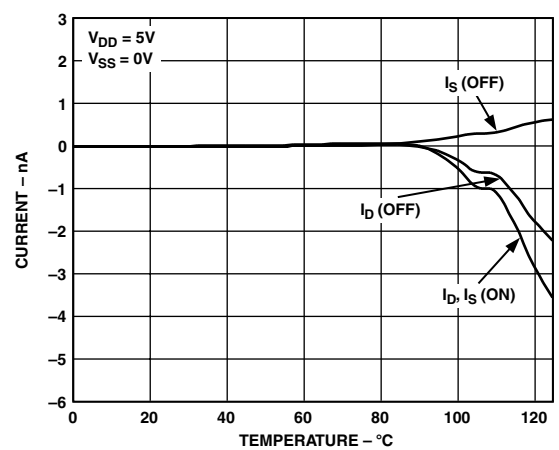
TPC 2. On Resistance vs. V_D (V_S), Single Supply



TPC 5. Leakage Currents vs. Temperature, Dual Supply

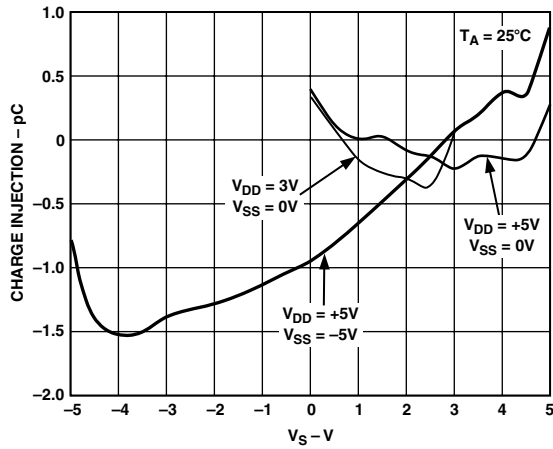


TPC 3. On Resistance vs. V_D (V_S) for Different Temperatures, Dual Supply

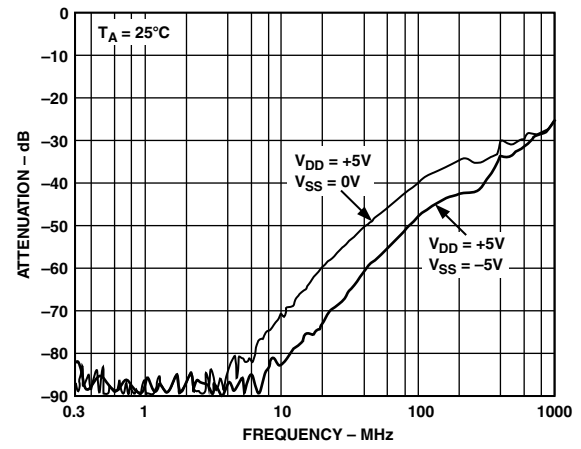


TPC 6. Leakage Currents vs. Temperature, Single Supply

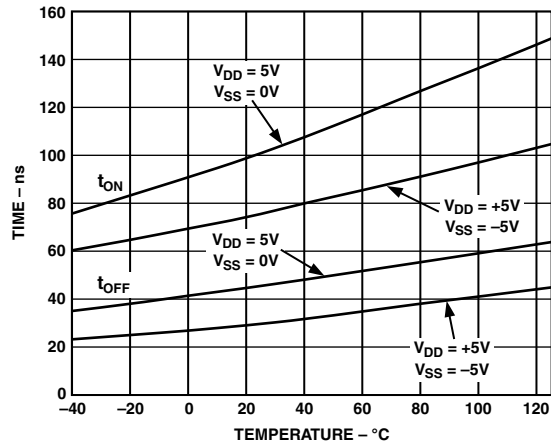
ADG604



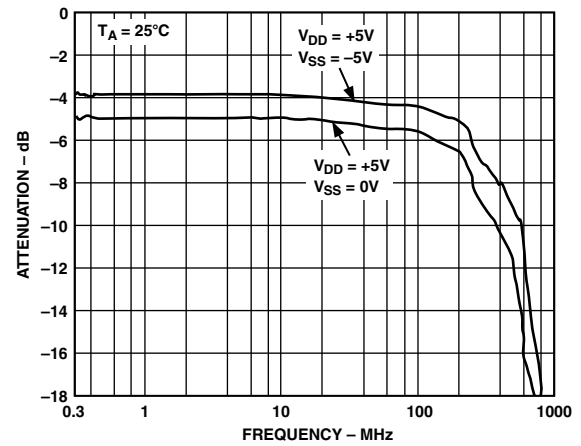
TPC 7. Charge Injection vs. Source Voltage



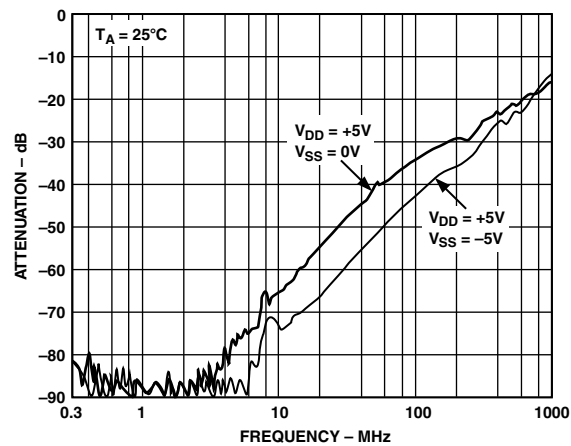
TPC 10. Crosstalk vs. Frequency



TPC 8. t_{ON}/t_{OFF} Times vs. Temperature

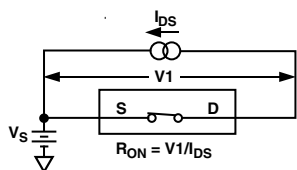


TPC 11. On Response vs. Frequency

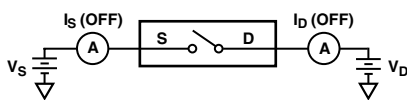


TPC 9. Off Isolation vs. Frequency

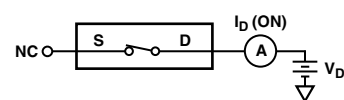
Test Circuits



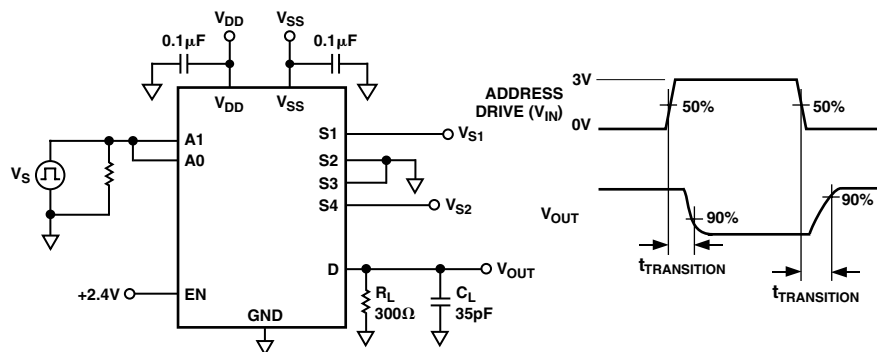
Test Circuit 1. On Resistance



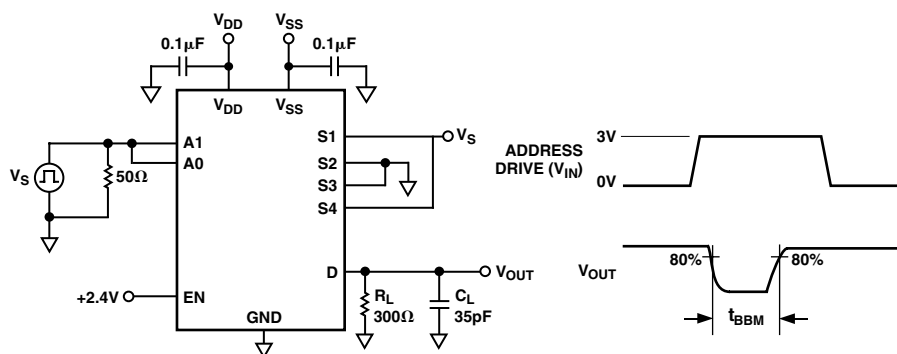
Test Circuit 2. Off Leakage



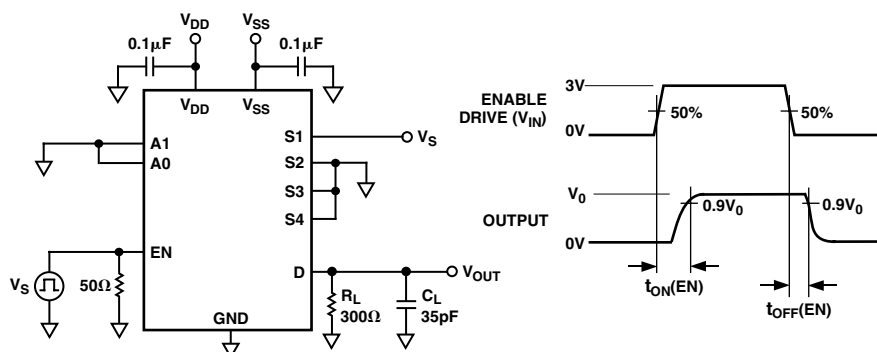
Test Circuit 3. On Leakage



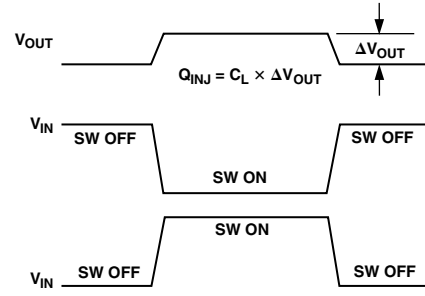
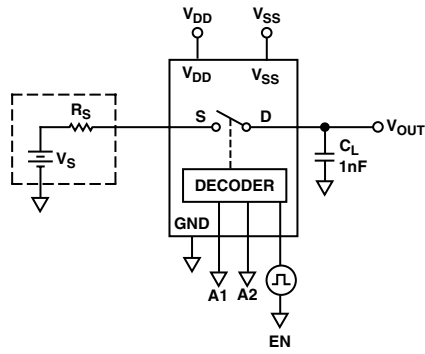
Test Circuit 4. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$



Test Circuit 5. Break-Before-Make Delay, t_{BBM}



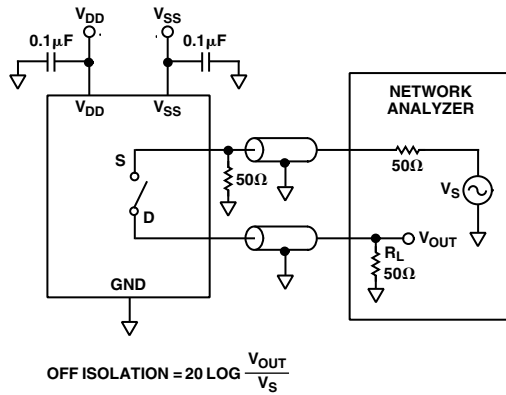
Test Circuit 6. Enable Delay, $t_{\text{ON}}(\text{EN})$, $t_{\text{OFF}}(\text{EN})$



$$Q_{INJ} = C_L \times \Delta V_{OUT}$$

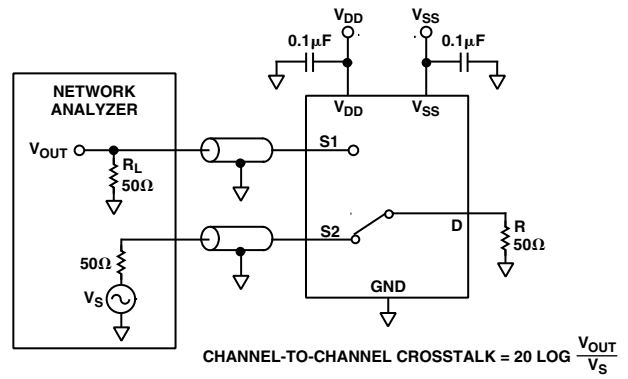
$$\text{CHARGE INJECTION} = \Delta V_{OUT} \times C_L$$

Test Circuit 7. Charge Injection



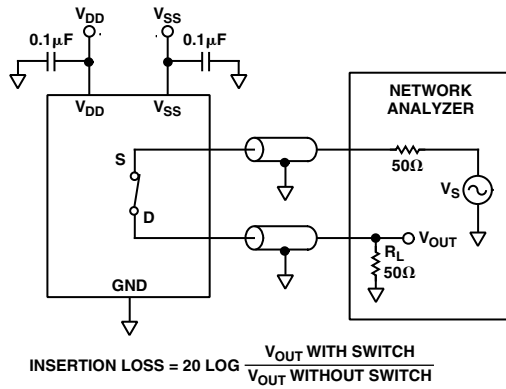
$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

Test Circuit 8. Off Isolation



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

Test Circuit 10. Channel-to-Channel Crosstalk



$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_{OUT \text{ WITHOUT SWITCH}}}$$

Test Circuit 9. Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**14-Lead TSSOP Package
(RU-14)**