DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4059
Programmable divide-by-n counter

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC06

1998 Jul 08

Philips
Semiconductors

PHILIPS

Programmable divide-by-n counter 74HC/HCT4059

FEATURES

- Synchronous programmable divide-by-n counter
- Presettable down counter
- Fully static operation
- Mode select control of initial decade counting function (divide-by-10, 8, 5, 4 and 2)
- Master preset initialization
- Latchable output
- Easily cascadable with other counters
- Four operating modes:
  timer
  divider-by-n
  divide-by-10 000
  master preset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4059 are high-speed Si-gate CMOS devices and are pin compatible with the “4059” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4059 are divide-by-n counters which can be programmed to divide an input frequency by any number (n) from 3 to 15 999. There are four operating modes, timer, divide-by-n, divide-by-10 000 and master preset, which are defined by the mode select inputs (K_a to K_c) and the latch enable input (LE) as shown in the Function table.

The complete counter consists of a first counting stage, an intermediate counting stage and a fifth counting stage. The first counter stage consists of four independent flip-flops. Depending on the divide-by-mode, at least one flip-flop is placed at the input of the intermediate stage (the remaining flip-flops are placed at the fifth stage with a place value of thousands). The intermediate stage consists of three cascaded decade counters, each containing four flip-flops.

All flip-flops can be preset to a desired state by means of the JAM inputs (J_1 to J_{16}), during which the clock input (CP) will cause all stages to count from n to zero. The zero-detect circuit will then cause all stages to return to the JAM count, during which an output pulse is generated. In the timer mode, after an output pulse is generated, the output pulse remains HIGH until the latch input (LE) goes LOW. The counter will advance, even if LE is HIGH and the output is latched in the HIGH state.

In the divide-by-n mode, a clock cycle wide pulse is generated with a frequency rate equal to the input frequency divided by n.

The function of the mode select and JAM inputs are illustrated in the following examples. In the divide-by-2 mode, only one flip-flop is needed in the first counting section. Therefore the last (5th) counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. This counting mode is selected when K_a to K_c are set HIGH. In this case input J_1 is used to preset the first counting section and J_2 to J_4 are used to preset the last (5th) counting section.

If the divide-by-10 mode is desired for the first section, K_a and K_b are set HIGH and K_c is set LOW. The JAM inputs J_1 to J_4 are used to preset the first counting section (there is no last counting section). The intermediate counting section consists of three cascaded BCD decade (divide-by-10) counters, presettable by means of the JAM inputs J_5 to J_{16}.

The preset of the counter to a desired divide-by-n is achieved as follows:

n = (MODE(1)) (1 000 x decade 5 preset
+ 100 x decade 4 preset
+ 10 x decade 3 preset
+ 1 x decade 2 preset)
+ decade 1 preset

To calculate preset values for any “n” count, divide the “n” count by the selected mode. The resultant is the corresponding preset value of the 5th to the 2nd decade with the remainder being equal to the 1st decade value; preset value = n/mode.

If n = 8 479, and the selected mode = 5, the preset value = 8 479/5 = 1 695 with a remainder of 4, thus the JAM inputs must be set as shown in Table 1.

To verify the results, use the given equation:

$n = 5\ (1\ 000 \times 1 + 100 \times 6 + 10 \times 9 + 1 \times 5) + 4$

n = 8 479.

If n = 12 382 and the selected mode = 8, the preset value = 12 382/8 = 1 547 with a remainder of 6, thus the JAM inputs must be set as shown in Table 2.

To verify:

$n = 8\ (1\ 000 \times 1 + 100 \times 5 + 10 \times 4 + 1 \times 7) + 6$

n = 12 382.

(1) MODE = first counting section divider (10, 8, 5, 4 or 2).

If n = 8 479 and the selected mode = 10, the preset value = 8 479/10 with a remainder of 9, thus the JAM inputs must be set as shown in Table 3.

To verify:

$n = 10\ (1\ 000 \times 0 + 100 \times 8 + 10 \times 4 + 1 \times 7) + 9$

n = 8 479.

The three decades of the intermediate counting section can be preset to a binary 15 instead of a BCD 9. In this case the first cycle of a counter consists of 15 count pulses, the next cycles consisting of 10 counting pulses. Thus the place value of the three decades are still 1, 10 and 100. For example, in the divide-by-8 mode, the number from which the intermediate counting section begins to count-down can be preset to:

3rd decade: 1 500
2nd decade: 150
1st decade: 15

The last counting section can be preset to a maximum of 1, with a place value of 1 000. The first counting section can be preset to a maximum of 7. To calculate n:

$n = 8\ (1\ 000 \times 1 + 100 \times 15 + 10 \times 15 + 1 \times 15) + 7$

n = 21 327.

21 327 is the maximum possible count in the divide-by-8 mode. The highest count of the various modes is shown in the Function table, in the column entitled “binary counter range”.

The mode select inputs permit, when used with decimal programming, a non-BCD least significant digit. For example, the channel spacing in a radio is 12.5 kHz, it may be convenient to program the counter in decimal steps of 100 kHz subdivided into 8 steps of 12.5 kHz controlled by the least significant digit. Also frequency synthesizer channel separations of 10, 12.5, 20, 25 and 50 parts can be chosen by the mode select inputs. This is called “Fractional extension”. A similar extension called “Half channel offset” can be obtained in modes 2, 4, 6 and 8, if the JAM inputs are switched between zero and 1, 2, 3 and 4 respectfully. This is illustrated in Fig.5.

This feature is used primarily in cases where radio channels are allocated according to the following formula:

Channel frequency = channel spacing x (N + 0.5)

N is an integer.

Control inputs K_b and K_c can be used to initiate and lock the counter in the “master preset” mode. In this condition the flip-flops in the counter are preset in accordance with the JAM inputs and the counter remains in that mode as long as K_b and K_c both remain LOW. The counter begins to count down from the preset state when a counting mode other than the “master preset” mode is selected. Whenever the “master preset” mode is used, control signals $K_b = K_c$ = LOW must be applied for at least 2 full clock pulses. After the “master preset” mode inputs have been changed to one of the counting modes, the next positive-going clock transition changes an internal flip-flop so that the count-down begins on the second positive-going clock transition. Thus, after a “master preset” mode, there is always one extra count before the output goes HIGH. Figure 6 illustrates the operation of the counter in the divide-by-8 mode starting from the preset state 3.

If the “master preset” mode is started two clock cycles or less before an output pulse, the output pulse will appear at the correct moment. When the output pulse appears and the “master preset” mode is not selected, the counter is preset according to the states of the JAM inputs.

When K_a, K_b, K_c and LE are LOW, the counter operates in the “preset inhibit” mode, during which the counter divides at a fixed rate of 10 000, independent of the state of the JAM inputs. However, the first cycle length after leaving the “master preset” mode is determined by the JAM inputs.

When K_a, K_b and K_c are LOW and input LE = HIGH, the counter operates in the normal divide-by-10 mode, however, without the latch operation at the output.

This device is particularly advantageous in digital frequency synthesizer circuits (VHF, UHF, FM, AM etc.) for communication systems, where programmable divide-by-”n” counters are an integral part of the synthesizer phase-locked-loop sub-system. The 74HC/HCT4059 can also be used to perform the synthesizer “fixed divide-by-n” counting function, as well as general purpose counting for instrumentation functions such as totalizers, production counters and “time out” timers.

Schmitt-trigger action at the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay CP to Q	C_L = 15 pF; V_{CC} = 5 V	18	20	ns
f_{max}	maximum clock frequency		40	40	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	30	32	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}

   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
74HC4059N3; 74HCT4059N3	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
74HC4059N; 74HCT4059N	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
74HC4059D; 74HCT4059D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	LE	latch enable (active HIGH)
3, 4, 5, 6, 22, 21, 20, 19, 18, 17, 16, 15, 10, 9, 8, 7	J_1 to J_{16}	programmable JAM inputs (BCD)
12	GND	ground (0 V)
14, 13, 11	K_a to K_c	mode select inputs
23	Q	divide-by-n output
24	V_{CC}	positive supply voltage

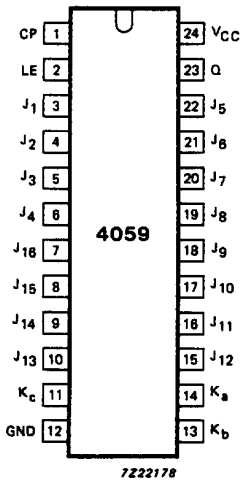


Fig.1 Pin configuration.

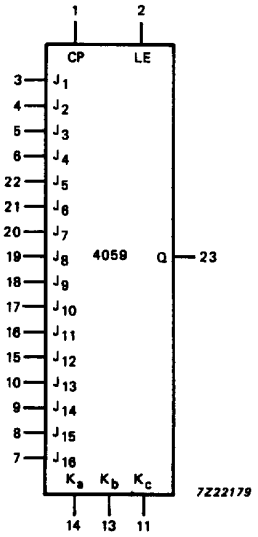


Fig.2 Logic symbol.

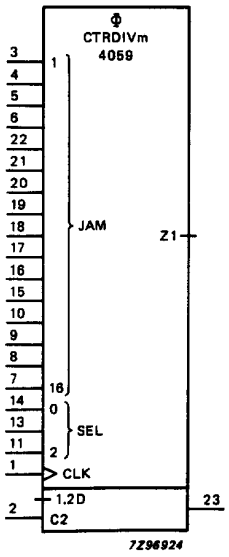


Fig.3 IEC logic symbol.

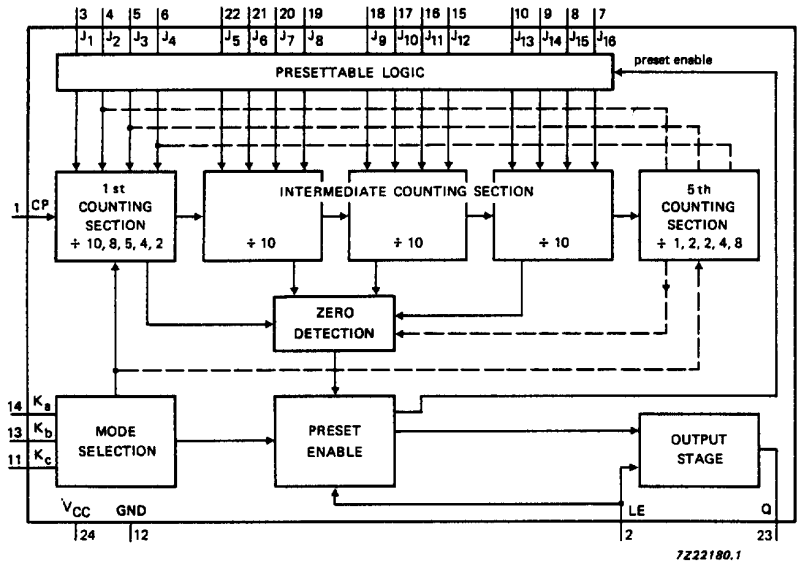


Fig.4 Functional block diagram.

APPLICATIONS

- Frequency synthesizer, ideally suited for use with PC74HC/HCT4046A, PC74HC/HCT7046A and PC74HC/HCT9046A (PLLs)
- Fixed or programmable frequency division
- “Time out” timer

FUNCTION TABLE

LATCH ENABLE INPUT	MODE SELECT INPUTS			FIRST COUNTING SECTION DECADE 1			LAST COUNTING SECTION DECADE 5			COUNTER RANGE		OPERATION
LE	K_a	K_b	K_c	MODE	MAX PRESET STATE	JAM INPUTS USED	DIVIDED BY	MAX. PRESET STATE	JAM INPUTS USED	BCD MAX.	BINARY MAX.	
H	H	H	H	2	1	J_1	8	7	$J_2J_3J_4$	15 999	17 331	timer mode
H	L	H	H	4	3	J_1J_2	4	3	J_3J_4	15 999	18 663	
H	H	L	H	5	4	$J_1J_2J_3$	2	1	J_4	9 999	13 329	
H	L	L	H	8	7	$J_1J_2J_3$	2	1	J_4	15 999	21 327	
H	H	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659	
L	H	H	H	2	1	J_1	8	7	$J_2J_3J_4$	15 999	17 331	divide-by-n mode
L	L	H	H	4	3	J_1J_2	4	3	J_3J_4	15 999	18 663	
L	H	L	H	5	4	$J_1J_2J_3$	2	1	J_4	9 999	13 329	
L	L	L	H	8	7	$J_1J_2J_3$	2	1	J_4	15 999	21 327	
L	H	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659	
H	L	H	L	10	9	$J_1J_2J_3J_4$	1	0	–	9 999	16 659	
L	L	H	L	preset inhibited			preset inhibited			fixed 10 000	–	divide-by-10 000 mode
X	X	L	L	master preset			master preset			–	–	master preset mode

Note

1. It is recommended that the device is in the master preset mode (K_b = K_c = logic 0) in order to correctly initialize the device prior to start-up. An example of a suitable external circuit is shown in Fig.14.
   H = HIGH voltage level
   L = LOW voltage level
   X = don't care

Table 1

4			1	5				9				6			
J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}	J_{15}	J_{16}
L	L	H	H	H	L	H	L	H	L	L	H	L	H	H	L

Table 2

6			1	7				4				5			
J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}	J_{15}	J_{16}
L	H	H	H	H	H	H	L	L	L	H	L	H	L	H	L

Table 3

9				7				4				8			
J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}	J_{15}	J_{16}
H	L	L	H	H	H	H	L	L	L	H	L	L	L	L	H

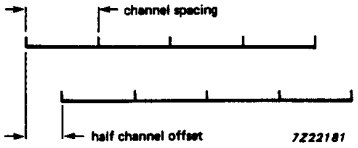


Fig.5 Half channel offset.

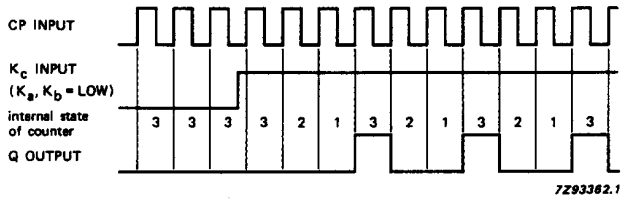


Fig.6 Total count of 3.

DC CHARACTERISTIC FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q		58	200		250		300	ns	2.0	Fig.7
			21	40		50		60		4.5	
			17	34		43		51		6.0	
t_{PHL}/ t_{PLH}	propagation delay LE to Q		50	175		220		265	ns	2.0	Fig.8
			18	35		44		53		4.5	
			14	30		37		45		6.0	
t_{THL}/ t_{TLH}	output transition time		19	75		95		110	ns	2.0	Fig.7
			7	15		19		22		4.5	
			6	13		16		19		6.0	
t_W	clock pulse width CP	90	7		115		135		ns	2.0	Fig.7
		18	6		23		27			4.5	
		15	5		90		23			6.0	
t_{rem}	removal time K_b, K_c to CP	75	19		95		110		ns	2.0	Fig.9; note 1
		15	7		19		22			4.5	
		13	6		16		19			6.0	
f_{max}	maximum clock pulse frequency	4.2	12		3.4		2.8		MHz	2.0	Fig.7
		21	36		17		14			4.5	
		25	43		20		17			6.0	

Note

1. From master preset mode to any other mode.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CP	0.65
LE	0.65
J_n	0.50
K_a	1.00
K_b	1.50
K_c	0.85

AC CHARACTERISTICS FOR 74HCT

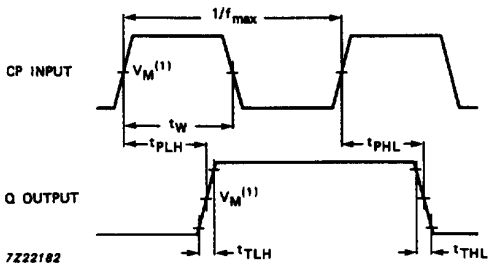
GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			–40 to +85		–40 to +125			V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q		24	46		58		69	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay LE to Q		24	46		58		69	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.7
t_W	clock pulse width CP	20	7		25		30		ns	4.5	Fig.7
t_{rem}	removal time K_b, K_c to CP	15	7		9		22		ns	4.5	Fig.9; note 1
f_{max}	maximum clock pulse frequency	21	36		17		14		MHz	4.5	Fig.7

Note

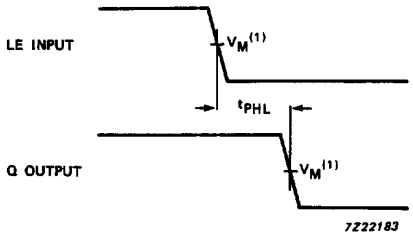
1. From master preset mode to any other mode.

AC WAVEFORMS



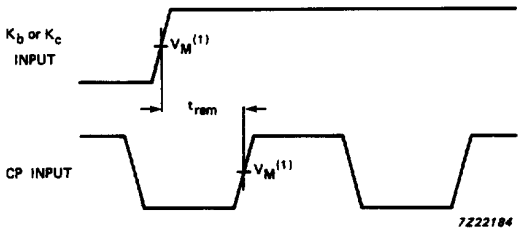
(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the clock (CP) to output (Q) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.



(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the LE input to Q output propagation delay.



(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the K_b or K_c removal times, when the operating mode is switched from master preset to any other mode.

APPLICATION INFORMATION

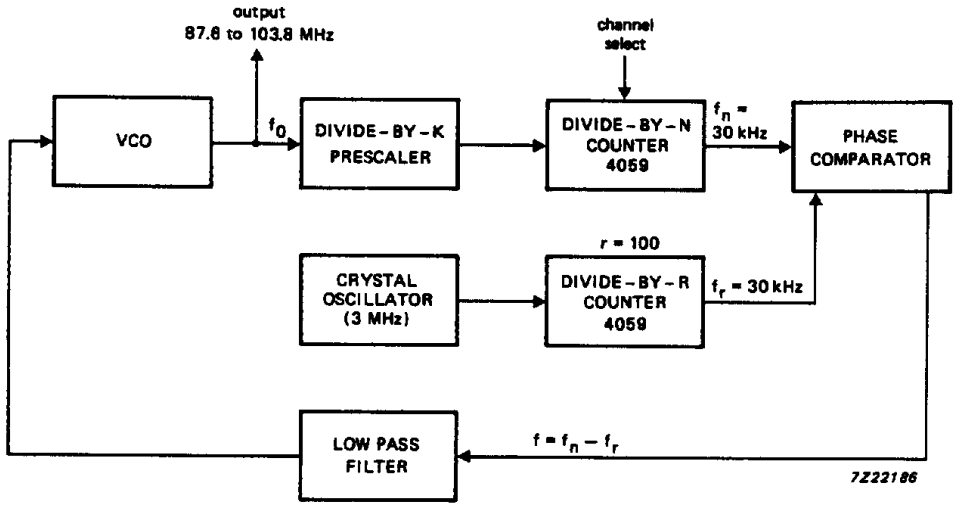


Fig.10 Example showing the application of the PC74HC/HCT4059 in a phase-locked-loop (PLL) for a FM band synthesizer.

Calculating the minimum and maximum divide-by-n values:

Output frequency range = 87.6 to 103.8 MHz (CCIR band 2)

Channel spacing frequency (f_c) = 300 kHz

Division factor prescaler (k) = 10

Reference frequency (f_r) = $\frac{f_c}{k} = \frac{300}{10} = 30$ kHz

Maximum divide-by-n value = $\frac{103.8\ \text{MHz}}{300\ \text{kHz}} = 346$

Minimum divide-by-n value = $\frac{87.6\ \text{MHz}}{300\ \text{kHz}} = 292$

Fixed divide-by-n value = $\frac{3\ \text{MHz}}{30\ \text{kHz}} = 100$

Application of the “4059” as divide-by-n counter allows programming of the channel spacing (shown in equations as 300 kHz). A channel in the CCIR band 2 is selected by the divide-by-n counter as follows:

channel = n – 290

Figure 11 shows a BCD switch compatible arrangement suitable for divide-by-5 and divide-by-8 modes, which can be adapted (with minimal changes) to the other divide-by-modes. In order to be able to preset to any number from 3 to 256 000, while preserving the BCD switch compatible character of the JAM inputs, a rather complex cascading scheme is necessary because the “4059” can never be preset to count less than 3. Logic circuitry is required to detect a condition where one of the numbers to be preset in the “4059” is < 3. In order to simplify the detection logic, only that condition is detected where the JAM inputs to terminals 6, 7 and 9 would be LOW during one count. If such a condition is detected, and if at least 1 is expected to be jammed into the MSB counter, the detection logic removes one from the number to be jammed into the MSB counter (with a place value of 2 000 times the divide-by-mode) and jams the same 2 000 into the “4059” by forcing pins 6, 7 and 9 HIGH.

The general circuit in Fig.11 can be simplified considerably if the range of the cascaded counters do not start at a very low value.

Figure 12 shows an arrangement in the divide-by-4 mode, where the counting range extends in a BCD switch compatible manner from 99 003 to 114 999.

The arrangement shown in Fig.12 is easy to follow; once during every cycle the programmed digits are jammed in (15 616 in this example) and then a round number of 11 000 is jammed in, nine times in succession, by forcing the JAM inputs via AND/OR gates.

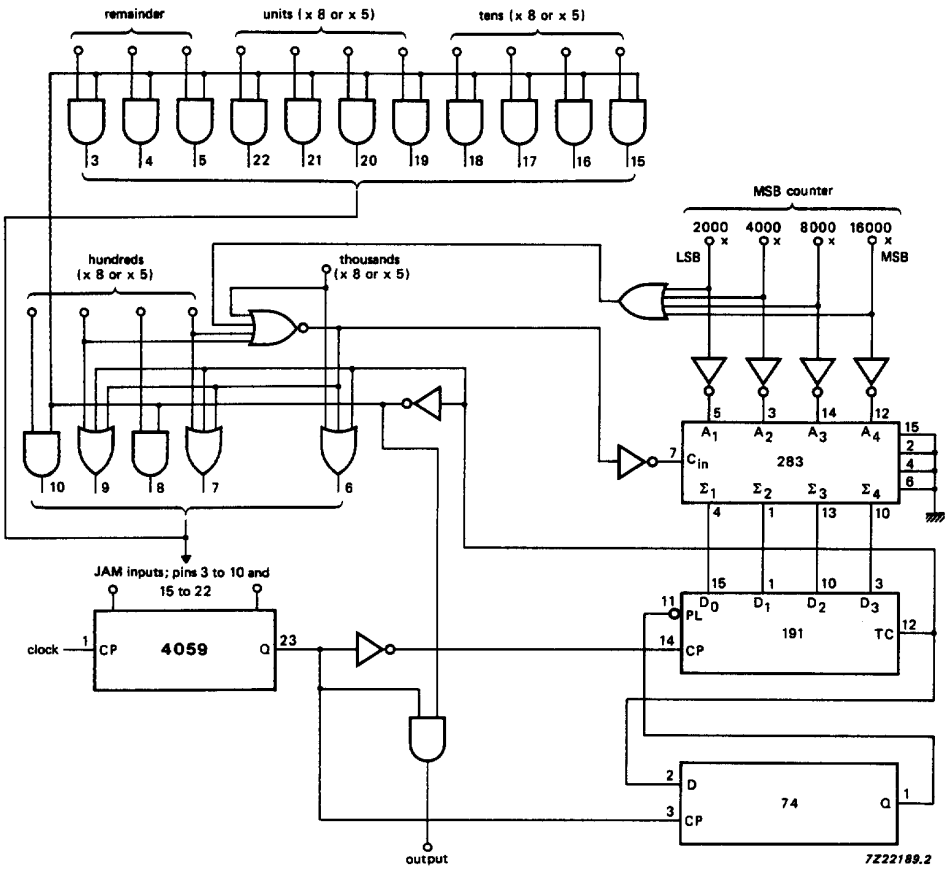
Numbers larger than the extended counter range can also be produced by cascading the PC74HC/HCT4059 with some other counting devices. Figure 13 shows such an arrangement where only one fixed divide-by number is desired. The dual flip-flop wired to produce a divide-by-3 count can be replaced by other counters such as the “190”, “191”, “192”, “193”, “4017”, “4510” and “4516”.

In Fig.13 the divide-by-n sub-system is preset once to a number which represents the least significant digits of the divide-by number (15 690 in the example shown in Fig.13). The sub-system is then preset twice to a round number (8 000 in the example shown in Fig.13) and multiplied by the number of the divide-by mode (2 in the example shown in Fig.13).

To verify:

$15\ 690 + 2 \times 8\ 000 \times 2 = 47\ 690$.

It is important that the second counting device has an output that is HIGH or LOW during only one of its counting states.



Each AND gate is 1/4 of PC74HC/HCT08.
Each OR gate is 1/3 of PC74HC/HCT4075.
Each NOR gate is 1/2 of PC74HC/HCT4002.
Each inverter is 1/6 of PC74HC/HCT04.

Fig.11 BCD switch compatible divide-by-n system suitable for divide-by-5 and divide-by-8 mode. Divides by any number from 3 to 256 000.

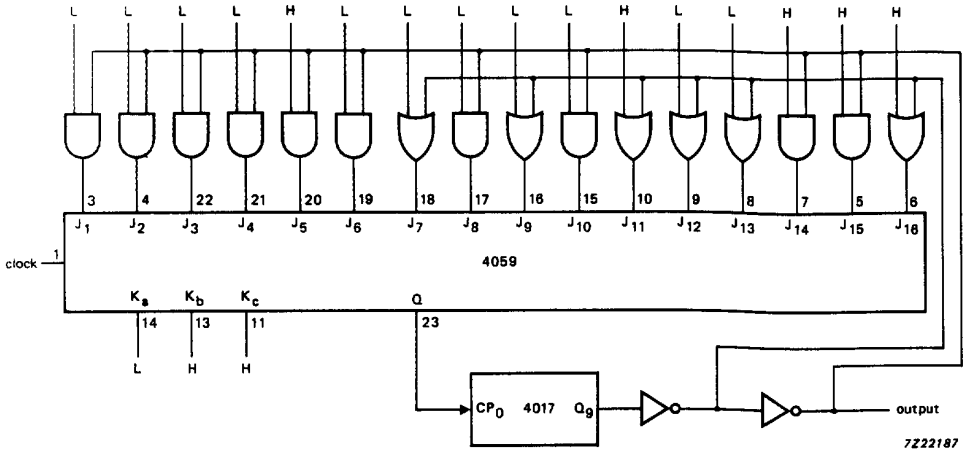


Fig.12 Dividing-by any number from 99 003 to 114 999 (in this example n = 114 616).

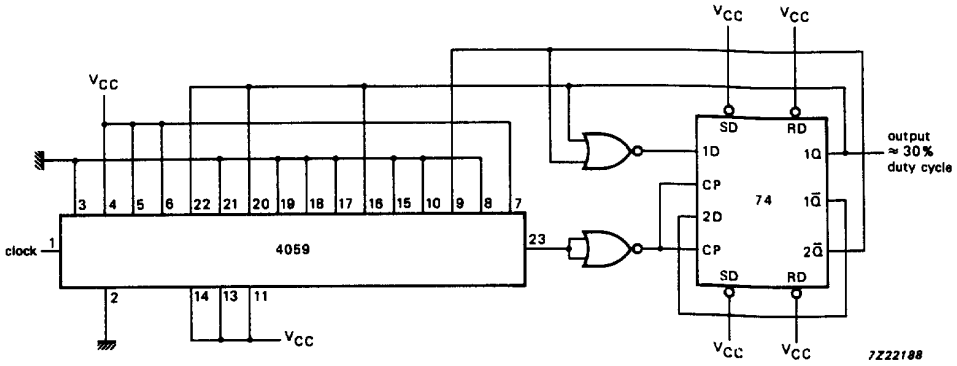


Fig.13 Division by 47 690 in divide-by-2 mode.

(1) $$RC \geq \frac{1}{0.2 \times f_{CP}(Hz)}$$

(2) It is assumed that the f_{CP} starts directly after the power-on. Any additional delay in starting f_{CP} must be added to the RC time.

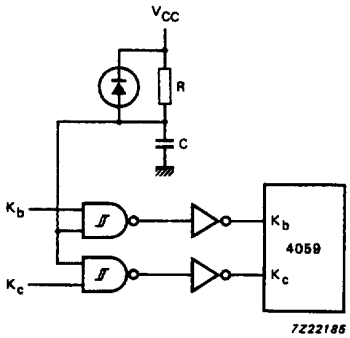
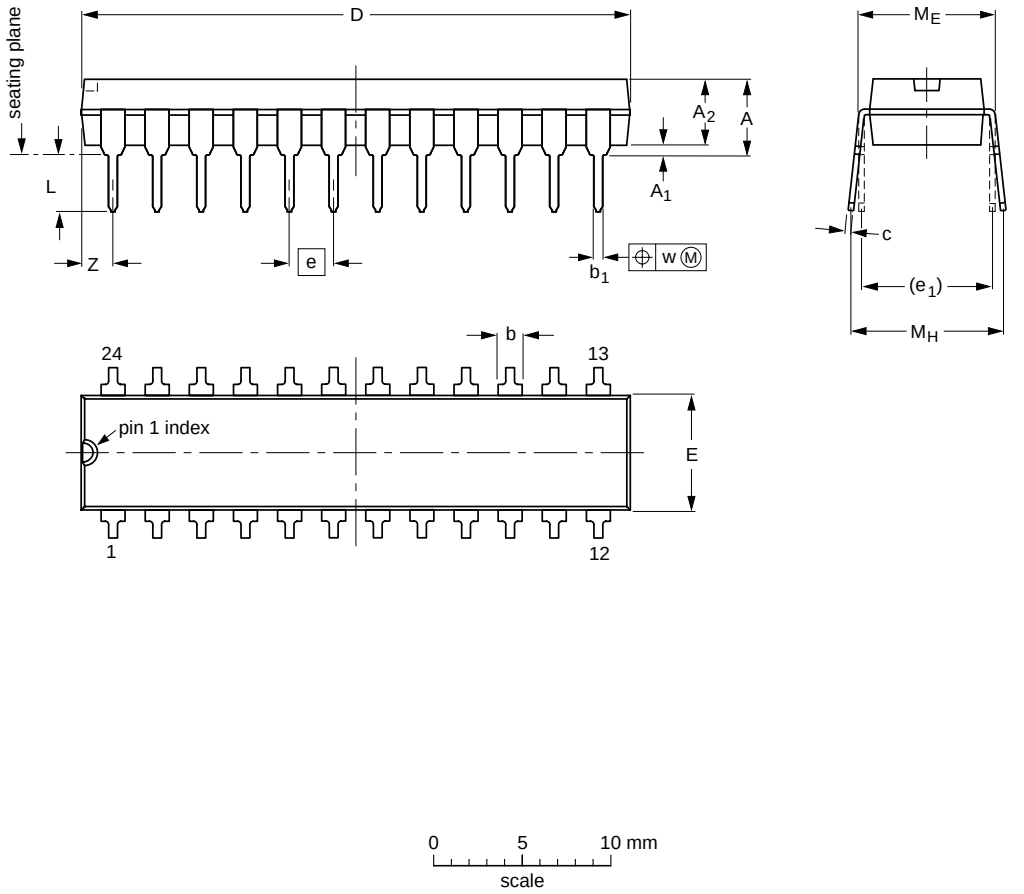


Fig.14 External circuit for master preset at start-up.

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

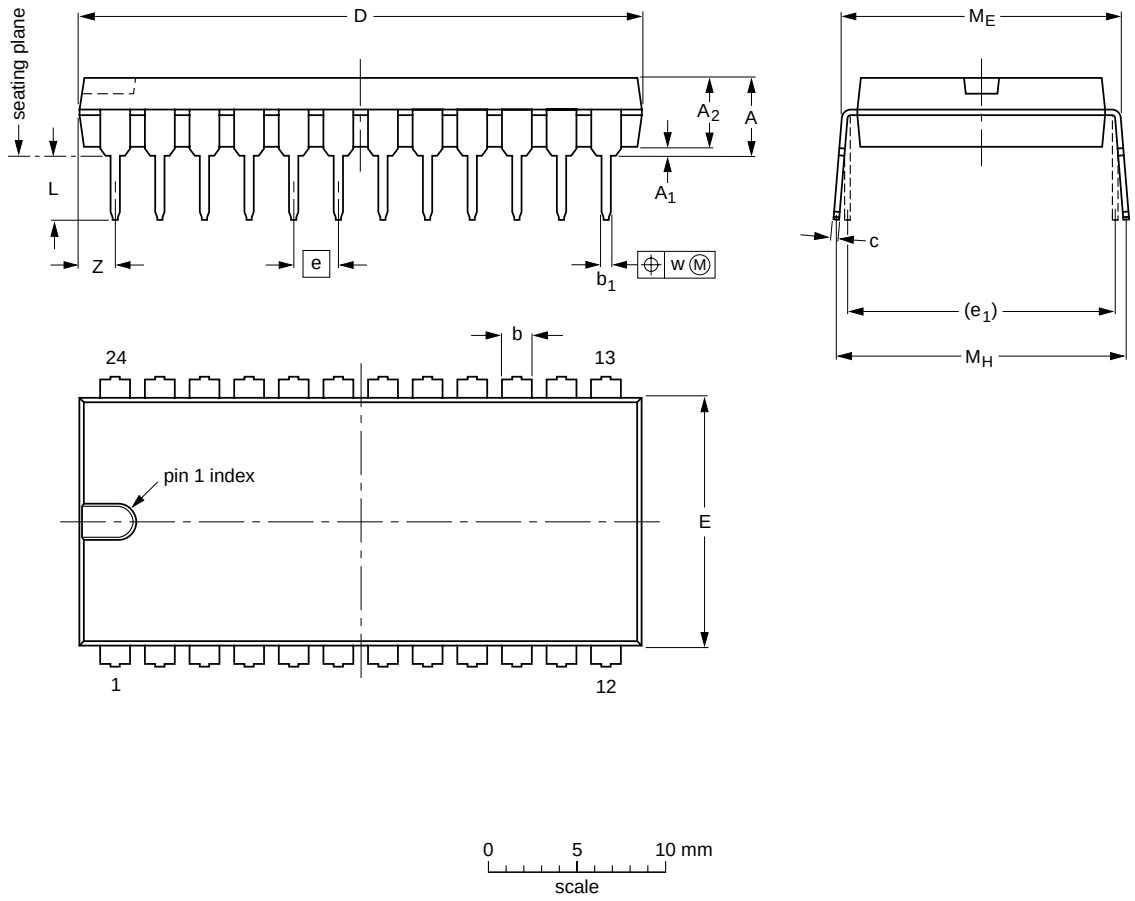
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

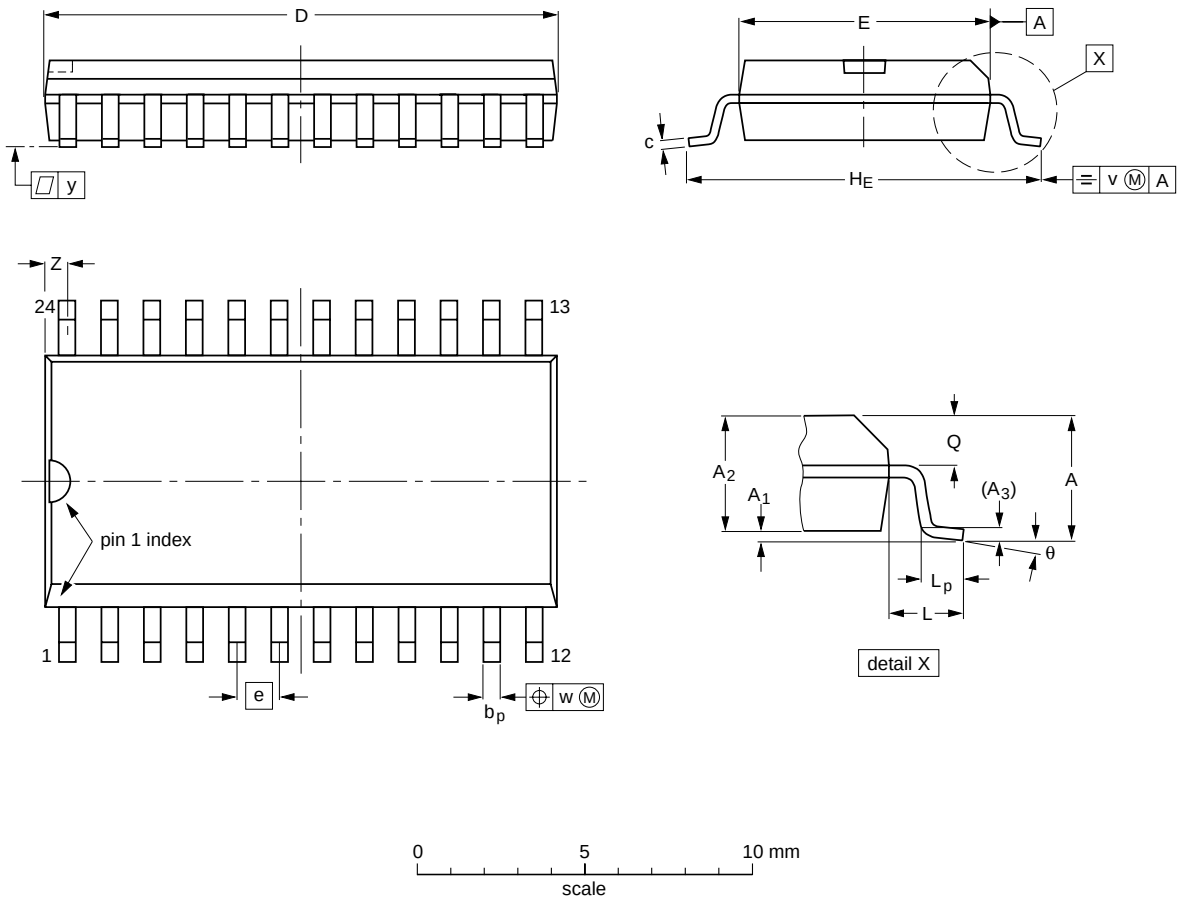
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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