

TLC7628C

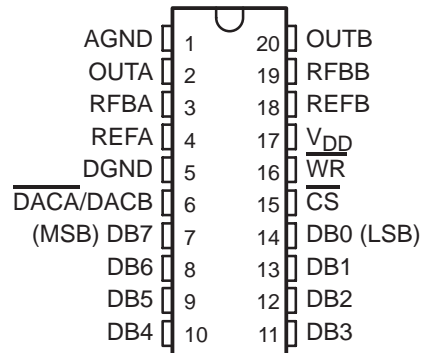
DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SLAS063B – APRIL 1989 – REVISED MARCH 2007

- Easy Microprocessor Interface
- On-Chip Data Latches
- Digital Inputs Are TTL-Compatible With 10.8-V to 15.75-V Power Supply
- Monotonic Over the Entire A/D Conversion Range
- Fast Control Signaling for Digital Signal Processor (DSP) Applications Including Interface With TMS320
- CMOS Technology

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation	20 mW
Settling Time	100 ns
Propagation Delay Time	80 ns

DW OR N PACKAGE
(TOP VIEW)



description

The TLC7628C is a dual, 8-bit, digital-to-analog converter (DAC) designed with separate on-chip data latches and featuring exceptionally close DAC-to-DAC matching. Data are transferred to either of the two DAC data latches through a common, 8-bit input port. Control input $\overline{\text{DACA/DACB}}$ determines which DAC is loaded. The load cycle of this device is similar to the write cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The TLC7628C operates from a 10.8-V to 15.75-V power supply and is TTL-compatible over this range. 2- or 4-quadrant multiplying makes this device a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7628C is characterized for operation from 0°C to +70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

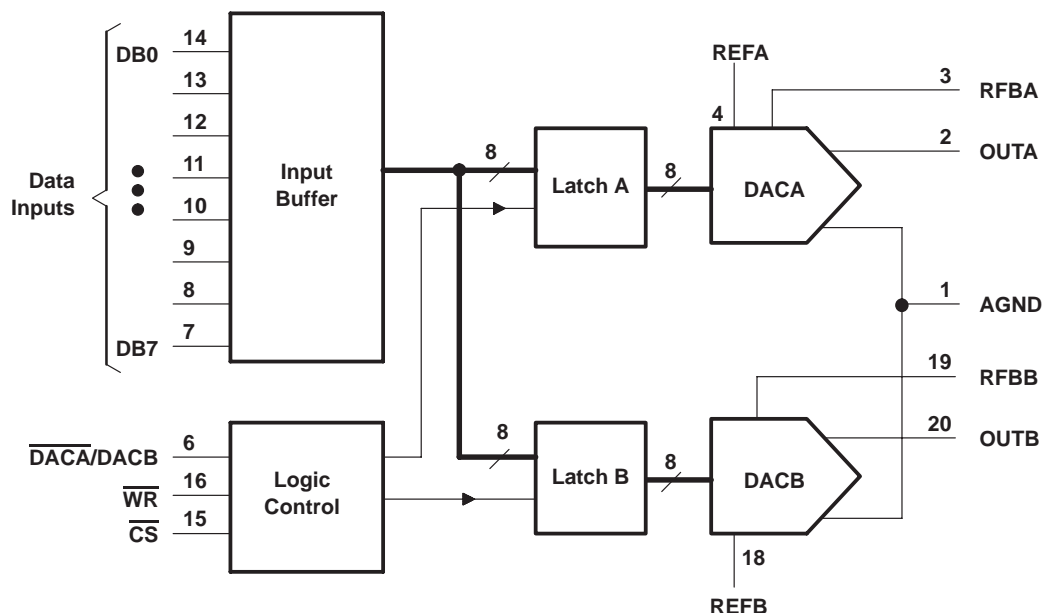
Copyright © 1995 – 2007, Texas Instruments Incorporated

TLC7628C

DUAL 8-BIT MULTIPLYING

SLAS063B – APRIL 1989 – REVISED MARCH 2007

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{DD} (to AGND or DGND)	–0.3 V to 17 V
Voltage between AGND and DGND	V_{DD}
Input voltage range, V_I (to DGND)	–0.3 V to $V_{DD} + 0.3$ V
Reference voltage range, V_{refA} or V_{refB} (to AGND)	± 25 V
Feedback voltage range, V_{RFBA} or V_{RFBB} (to AGND)	± 25 V
Output voltage range, V_{OA} or V_{OB} (to AGND)	± 25 V
Peak input current	10 μ A
Operating free-air temperature range, T_A : TLC7628C	0°C to +70°C
Storage temperature range, T_{stg}	–65°C to +150°C
Case temperature for 10 seconds, T_C : FN package	+260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	+260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	10.8		15.75	V
Reference voltage, V_{refA} or V_{refB}		± 10		V
High-level input voltage, V_{IH}	2.4			V
Low-level input voltage, V_{IL}			0.8	V
\overline{CS} setup time, $t_{su}(CS)$	50			ns
\overline{CS} hold time, $t_h(CS)$ (see Figure 1)	0			ns
DAC select setup time, $t_{su}(DAC)$ (see Figure 1)	60			ns
DAC select hold time, $t_h(DAC)$ (see Figure 1)	10			ns
Data bus input setup time $t_{su}(D)$ (see Figure 1)	25			ns
Data bus input hold time $t_h(D)$ (see Figure 1)	10			ns
Pulse duration, \overline{WR} low, $t_w(WR)$ (see Figure 1)	50			ns
Operating free-air temperature, T_A	TLC7628C			0 +70 °C

electrical characteristics over recommended ranges of operating free-air temperature and V_{DD} , $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
I _{IH}	High-level input current		V _I = V _{DD}	Full range		10	μA
				25°C		1	
I _{IL}	Low-level input current		V _I = 0	Full range		−10	μA
				25°C		−1	
Reference input impedance REFA or REFB to AGND					5	20	kΩ
I _{kg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, V _{refA} = ±10 V	Full range		±200	nA
				25°C		±50	
		OUTB	DAC data latch loaded with 00000000, V _{refB} = ±10 V	Full range		±200	
				25°C		±50	
Input resistance match (REFA to REFB)					±1%		
DC supply sensitivity Δgain/ΔV _{DD}			ΔV _{DD} = ± 5 %	Full range		0.02	%/%
				25°C		0.01	
I _{DD}	Supply current	Quiescent	All digital inputs at V _{IHmin} or V _{ILmax}			2	mA
		Standby	All digital inputs at 0 V or V _{DD}	Full range		0.5	
				25°C		0.1	
C _i	Input capacitance	DB0–DB7				10	pF
		WR, CS, DACA/DACB				15	
C _O	Output capacitance (OUTA, OUTB)	DAC data latches loaded with 00000000				25	pF
		DAC data latches loaded with 11111111				60	

TLC7628C

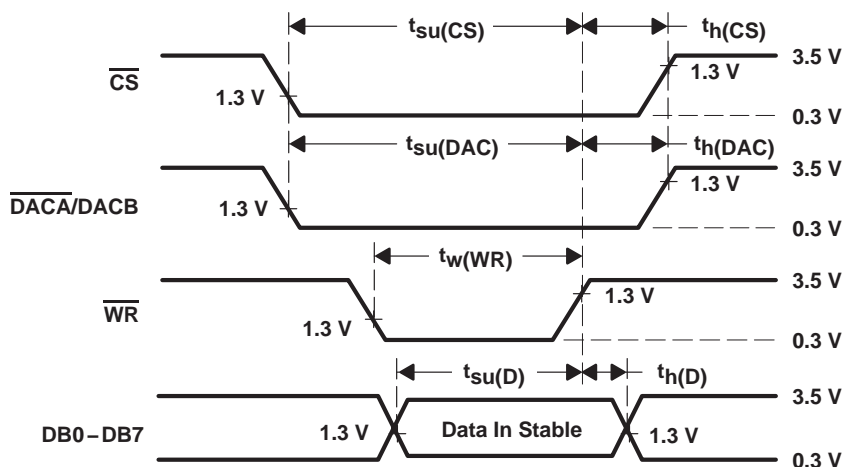
DUAL 8-BIT MULTIPLYING

SLAS063B – APRIL 1989 – REVISED MARCH 2007

operating characteristics over recommended ranges of operating free-air temperature and V_{DD} , $V_{refA} = V_{refB} = 10\text{ V}$, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Linearity error						$\pm 1/2$	LSB
Settling time (to 1/2 LSB)		See Note 1				100	ns
Gain error		See Note 2	Full range			± 3	LSB
			25°C			± 2	
AC feedthrough	REFA to OUTA	See Note 3	Full range			-65	dB
	REFB to OUTB		25°C			-75	
Temperature coefficient of gain						± 0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 4				80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 5	25°C		80		dB
	REFB to OUTA	See Note 6	25°C		80		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, $T_A = 25^\circ\text{C}$			330		nV•s
Digital crosstalk		Measured for code transition from 00000000 to 11111111, $T_A = 25^\circ\text{C}$			60		nV•s
Harmonic distortion		$V_i = 6\text{ V}$, $f = 1\text{ kHz}$, $T_A = 25^\circ\text{C}$				-85	dB

- NOTES: 1. OUTA, OUTB load = 100 Ω , $C_{ext} = 13\text{ pF}$; \overline{WR} and \overline{CS} at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal full scale range (FSR) = $V_{ref} - 1\text{ LSB}$. Both DAC latches are loaded with 11111111.
3. $V_{ref} = 20\text{ V}$ peak-to-peak, 10-kHz sine wave
4. $V_{refA} = V_{refB} = 10\text{ V}$; OUTA/OUTB load = 100 Ω , $C_{ext} = 13\text{ pF}$; \overline{WR} and \overline{CS} at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
5. $V_{refA} = 20\text{ V}$ peak-to-peak, 10-kHz sine wave; $V_{refB} = 0$
6. $V_{refB} = 20\text{ V}$ peak-to-peak, 10-kHz sine wave; $V_{refA} = 0$

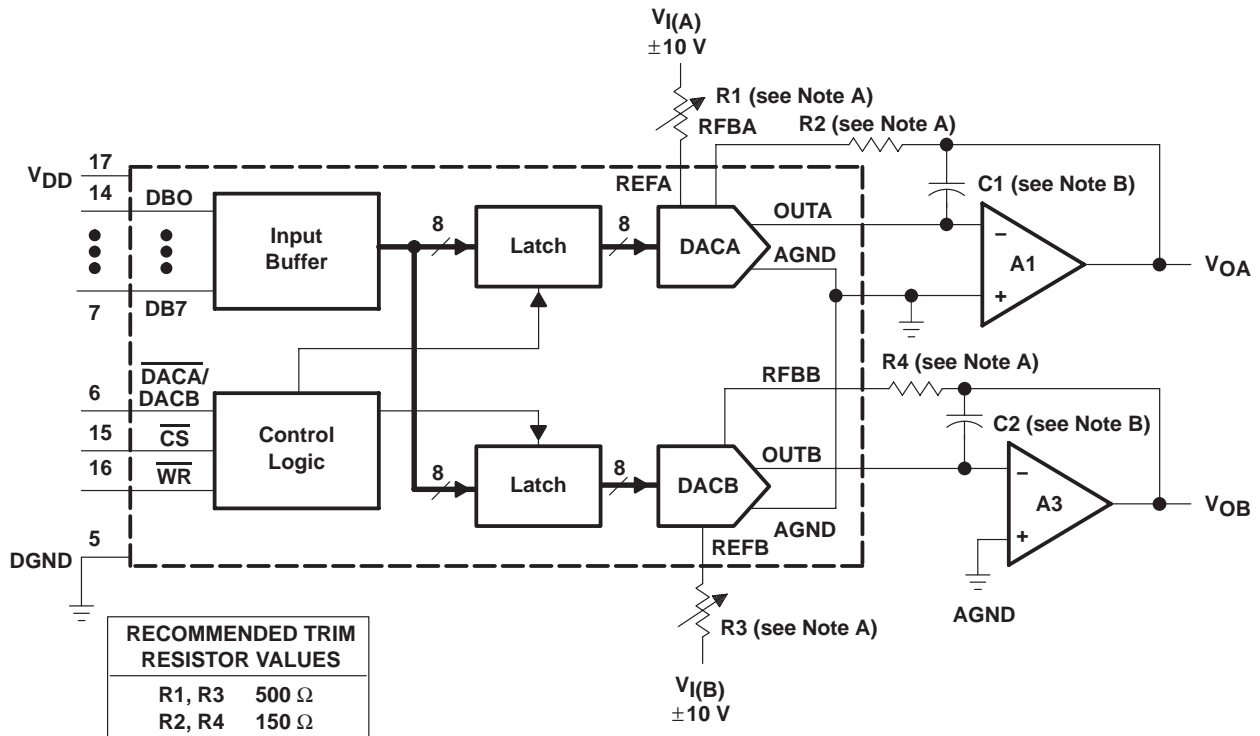


For all input signals, $t_r = t_f = 5\text{ ns}$ (10% to 90% points).

Figure 1. Setup and Hold Times

APPLICATION INFORMATION

This device is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 2 and 3, respectively.



- NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
- B. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

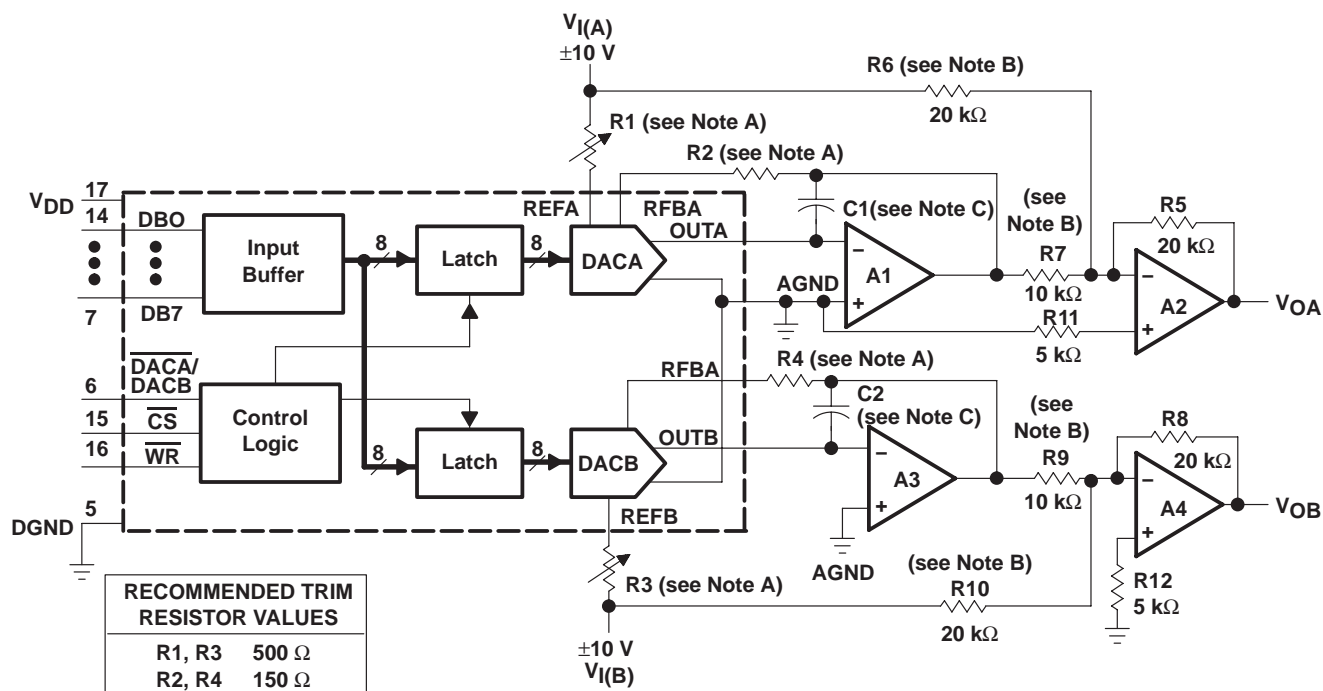
Figure 2. Unipolar Operation (2-Quadrant Multiplication)

TLC7628C

DUAL 8-BIT MULTIPLYING

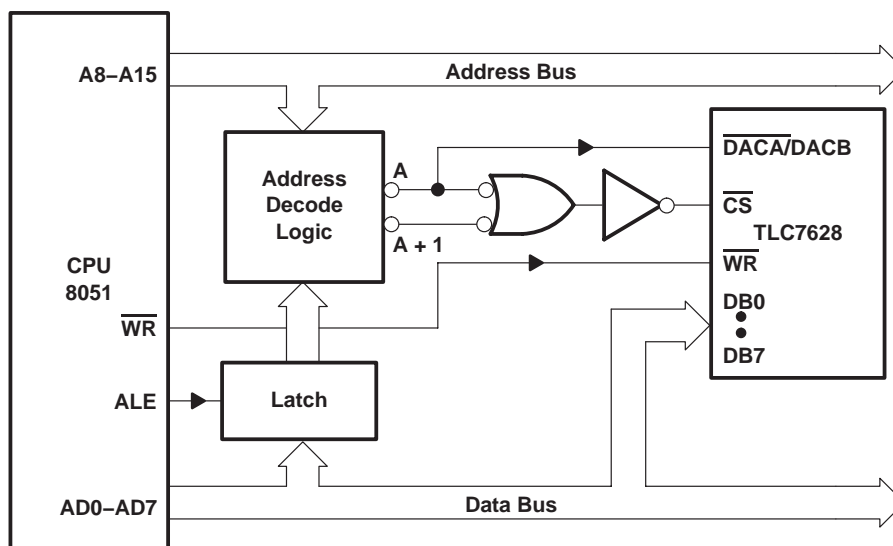
SLAS063B – APRIL 1989 – REVISED MARCH 2007

APPLICATION INFORMATION



- NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Adjust R1 for $V_{OA} = 0$ V with code 10000000 in DACA latch. Adjust R3 for $V_{OB} = 0$ V with 10000000 in DACB latch.
- B. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
- C. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

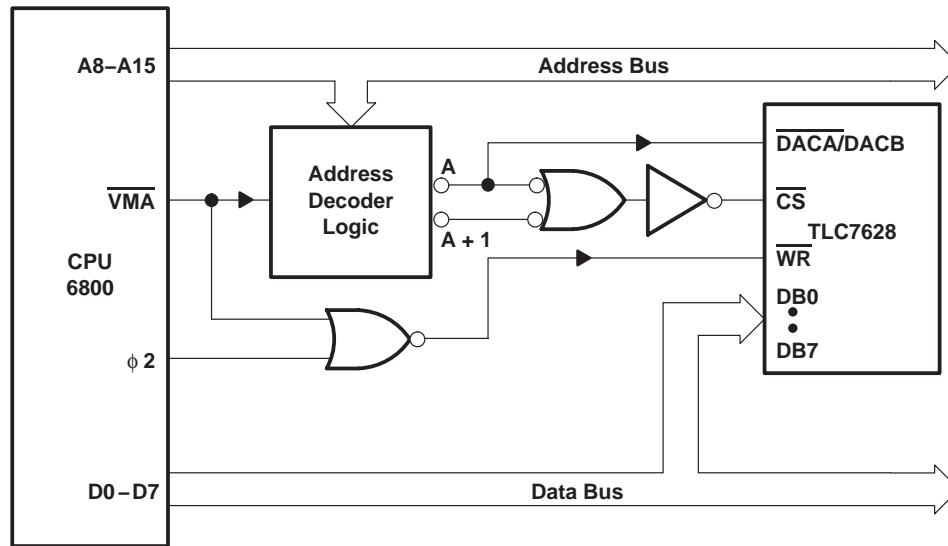
Figure 3. Bipolar Operation (4-Quadrant Operation)



NOTE D: A = decoded address for TLC7628 DACA
A + 1 = decoded address for TLC7628 DACB

Figure 4. TLC7628 — Intel 8051 Interface

APPLICATION INFORMATION



NOTE D: A = decoded address for TLC7628 DACA
A + 1 = decoded address for TLC7628 DACB

Figure 5. TLC7628 – 6800 Interface

voltage-mode operation

The current-multiplying DAC in the TLC7628C can be operated in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. An example of a current-multiplying DAC operating in voltage mode is shown in Figure 6. The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

$$\text{Analog output voltage} = \text{fixed input voltage} (D/256)$$

where D = the digital input. In voltage-mode operation, these devices meet the following specification:

LINEARITY ERROR	TEST CONDITIONS	MIN	MAX	UNIT
Analog output voltage for REFA, REFB	$V_{DD} = 12\text{ V}$, $OUTA$ or $OUTB$ at 5 V , $T_A = 25^\circ\text{C}$		1	LSB

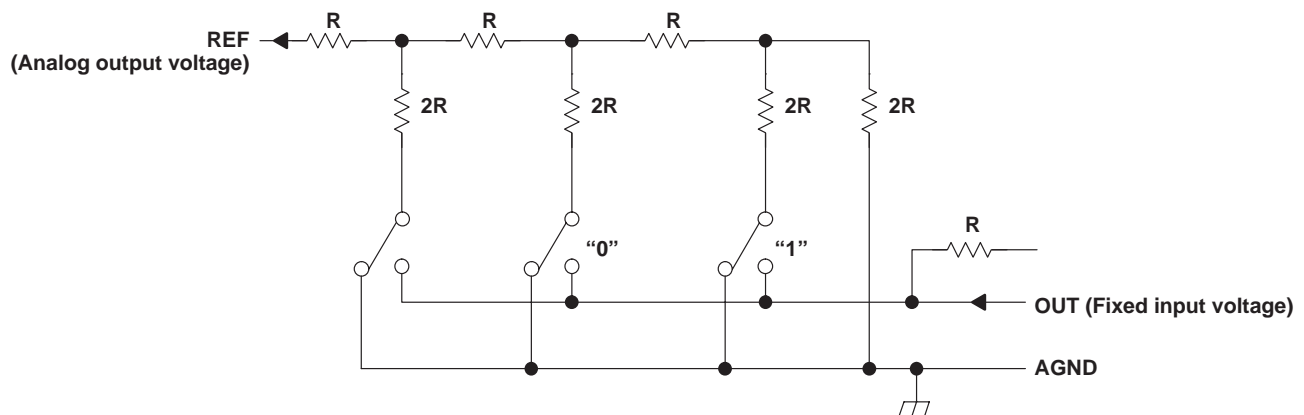


Figure 6. Current-Multiplying DAC Operating in Voltage Mode

TLC7628C

DUAL 8-BIT MULTIPLYING

SLAS063B – APRIL 1989 – REVISED MARCH 2007

PRINCIPLES OF OPERATION

This device contains two, identical, 8-bit, multiplying DACs: DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between the DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA or DACB with all digital inputs low is shown in Figure 7.

Figure 8 shows the DACA or DACB equivalent circuit. Both DACs share the analog ground terminal 1 (AGND). With all digital inputs high, the reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. The C_o is caused by the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_o is 25 pF to 60 pF maximum. The equivalent output resistance (r_o) varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

The TLC7628C interfaces to a microprocessor through the data bus, \overline{CS} , \overline{WR} , and $\overline{DACA/DACB}$ control signals. When \overline{CS} and \overline{WR} are both low, the analog output on this device, specified by the $\overline{DACA/DACB}$ control line, responds to the activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the \overline{CS} signal or \overline{WR} signal goes high, the data on the DB0–DB7 inputs are latched until the \overline{CS} and \overline{WR} signals go low again. When \overline{CS} is high, the data inputs are disabled, regardless of the state of the \overline{WR} signal.

The digital inputs of the TLC7628C provides TTL compatibility when operated from a supply voltage of 10.8 V to 15.75 V.

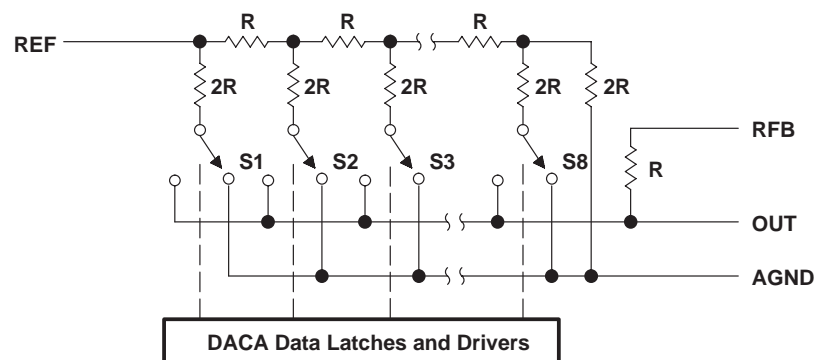


Figure 7. Simplified Functional Circuit for DACA or DACB

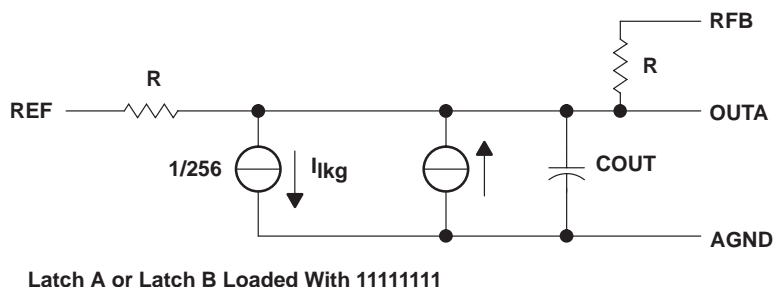


Figure 8. TLC7628 Equivalent Circuit for DACA or DACB

PRINCIPLES OF OPERATION

Table 1. Mode Selection Table

$\overline{\text{DACA/DACB}}$	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DACA	DACB
L	L	L	Write	Hold
H	L	L	Hold	Write
X	H	X	Hold	Hold
X	X	H	Hold	Hold

L = low level, H = high level, X = don't care

Table 2. Unipolar Binary Code

DAC LATCH CONTENTS (see Note 7)		ANALOG OUTPUT
MSB	LSB	
1	1	$-V_I (255/256)$
1	0	$-V_I (129/256)$
1	0	$-V_I (128/256) = -V_I/2$
0	1	$-V_I (127/256)$
0	0	$-V_I (1/256)$
0	0	$-V_I (0/256) = 0$

Table 3. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS (see Note 8)		ANALOG OUTPUT
MSB	LSB	
1	1	$V_I (127/128)$
1	0	$V_I (1/128)$
1	0	0 V
0	1	$-V_I (1/128)$
0	0	$-V_I (127/128)$
0	0	$-V_I (128/128)$

NOTES: 7. $1 \text{ LSB} = (2^{-8})V_I$
8. $1 \text{ LSB} = (2^{-7})V_I$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC7628CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7628C	Samples
TLC7628CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7628C	Samples
TLC7628CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC7628CN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7628CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7628CDWR	SOIC	DW	20	2000	367.0	367.0	45.0

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

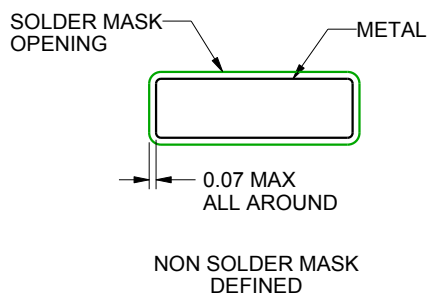
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Texas Instruments:](#)

[TLC7628CNE4](#)