

# HEF40193B

## 4-bit up/down binary counter

Rev. 8 — 18 November 2011

Product data sheet

### 1. General description

The HEF40193B is a 4-bit synchronous up/down binary counter. The counter has a count-up clock input (CPU), a count-down clock input (CPD), an asynchronous parallel load input ( $\overline{\text{PL}}$ ), four parallel data inputs (D0 to D3), an asynchronous master reset input (MR), four counter outputs (Q0 to Q3), an active LOW terminal count-up (carry) output ( $\overline{\text{TCU}}$ ), and an active LOW terminal count-down (borrow) output ( $\overline{\text{TCD}}$ ).

The counter outputs change state on the LOW-to-HIGH transition of either clock input. However, for correct counting, both clock inputs cannot be LOW simultaneously. The outputs  $\overline{\text{TCU}}$  and  $\overline{\text{TCD}}$  are normally HIGH. When the circuit has reached the maximum count state of '15', the next HIGH-to-LOW transition of CPU will cause  $\overline{\text{TCU}}$  to go LOW.  $\overline{\text{TCU}}$  will stay LOW until CPU goes HIGH again. Likewise, output  $\overline{\text{TCD}}$  will go LOW when the circuit is in the zero state and CPD goes LOW. When  $\overline{\text{PL}}$  is LOW, the information on D0 to D3 is asynchronously loaded into the counter. A HIGH on MR resets the counter independent of all other input conditions. The counter stages are of a static toggle type flip-flop.

It operates over a recommended  $V_{\text{DD}}$  power supply range of 3 V to 15 V referenced to  $V_{\text{SS}}$  (usually ground). Unused inputs must be connected to  $V_{\text{DD}}$ ,  $V_{\text{SS}}$ , or another input.

### 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Ordering information

**Table 1.** Ordering information

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Type number	Package		
	Name	Description	Version
HEF40193BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF40193BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



4. Functional diagram

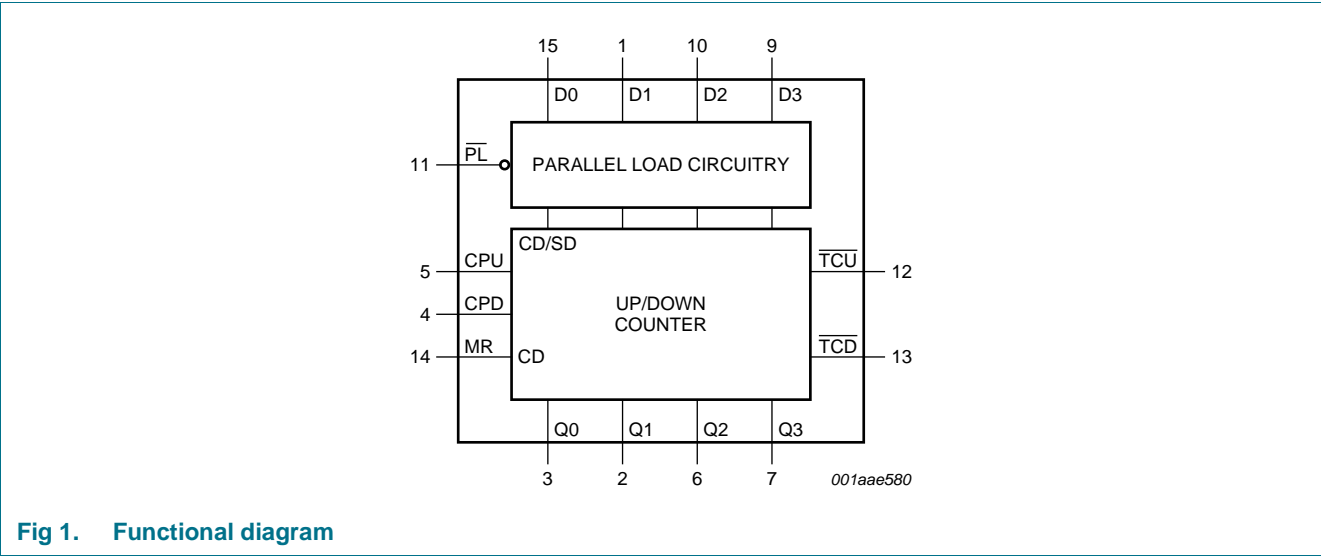
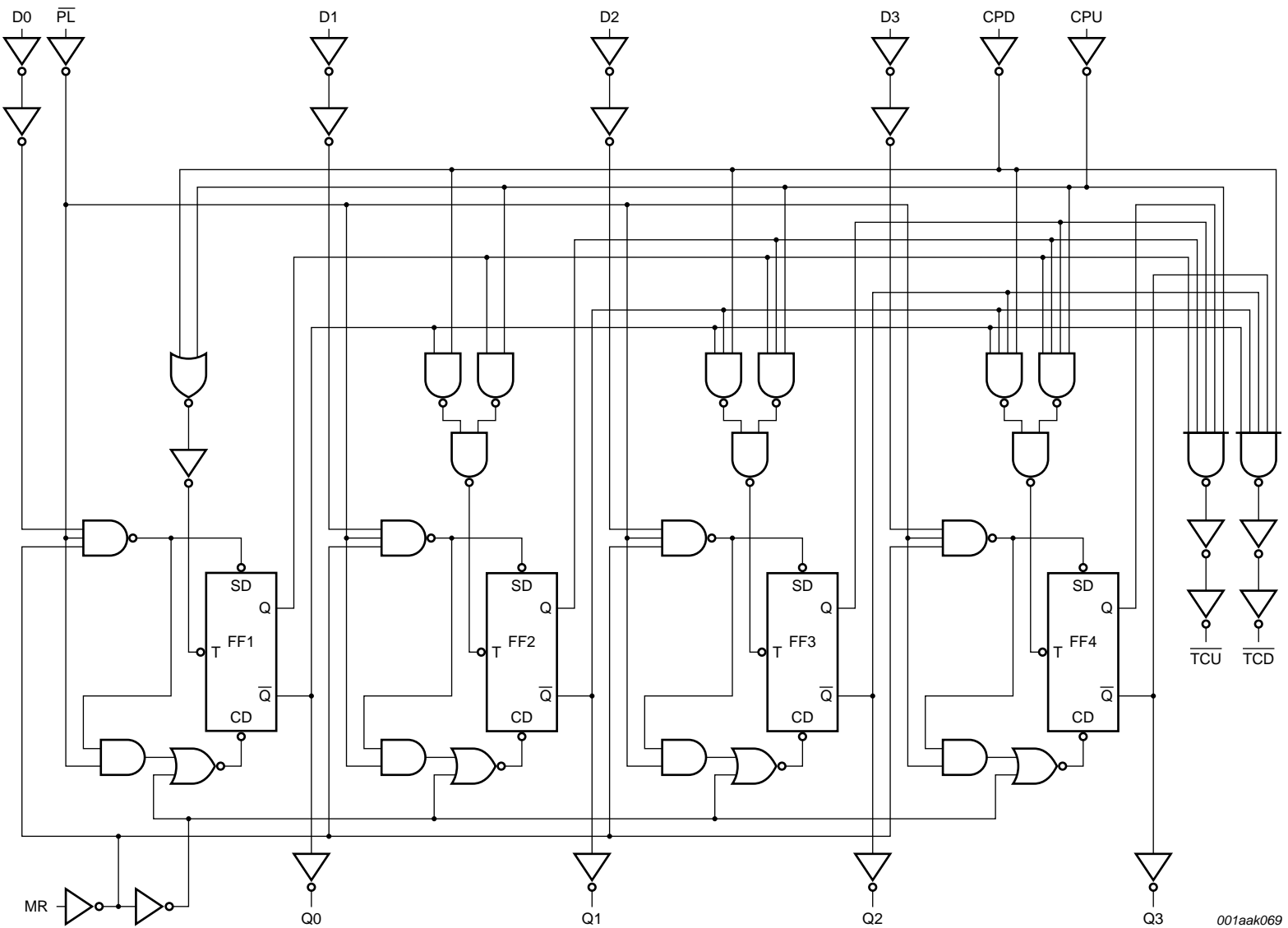


Fig 1. Functional diagram



**Fig 2. Logic diagram**

5. Pinning information

5.1 Pinning

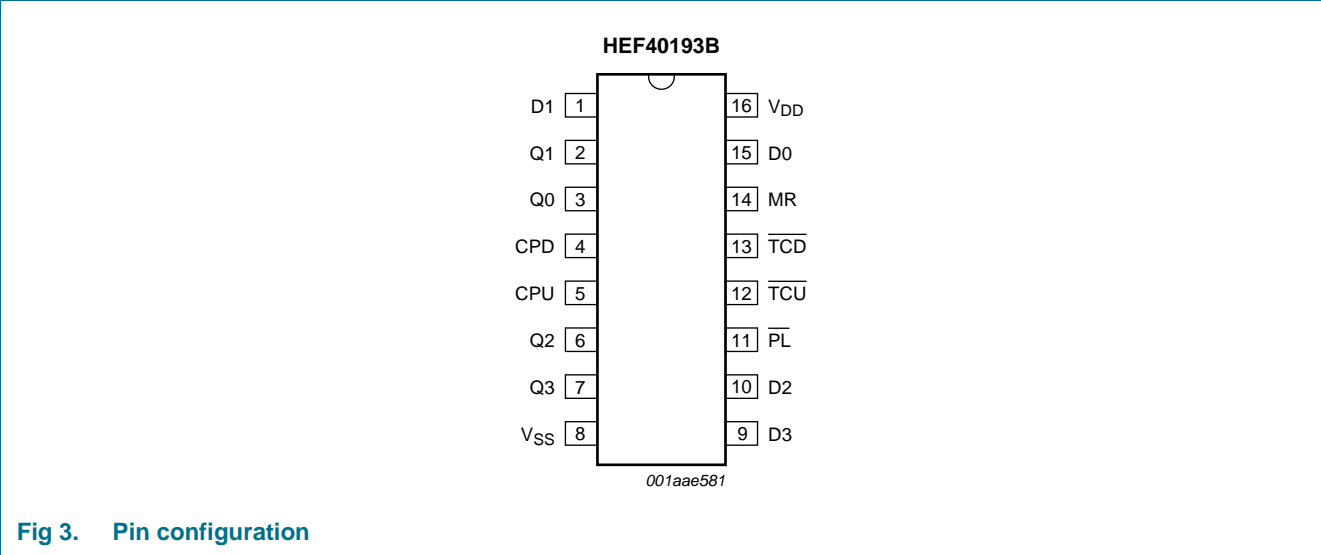


Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
D0 to D3	15, 1, 10, 9	parallel data input
CPU	5	count-up clock pulse input (LOW-to-HIGH, edge-triggered)
CPD	4	count-down clock pulse input (LOW-to-HIGH, edge-triggered)
PL	11	parallel load input (active LOW)
MR	14	master reset input (asynchronous)
Q0 to Q3	3, 2, 6, 7	buffered counter output
TCU	12	buffered terminal count-up (carry) output (active LOW)
TCD	13	buffered terminal count-down (borrow) output (active LOW)
V <sub>DD</sub>	16	supply voltage
V <sub>SS</sub>	8	ground supply voltage

6. Functional description

Table 3. Function table [1]

MR	PL	CPU	CPD	Mode
H	X	X	X	reset (asynchronous)
L	L	X	X	parallel load
L	H	↑	H	count-up
L	H	H	↑	count-down

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition.

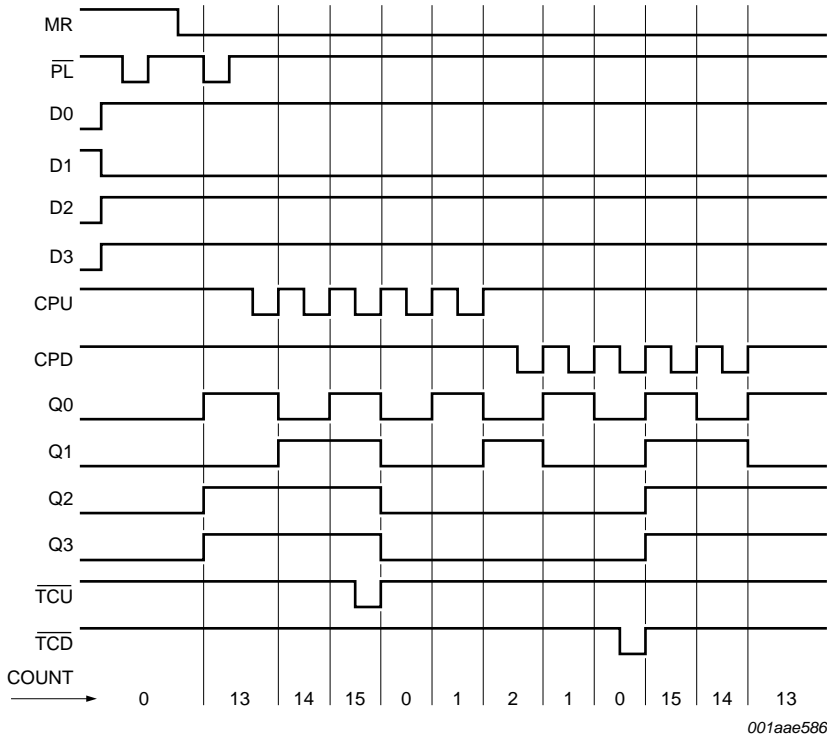
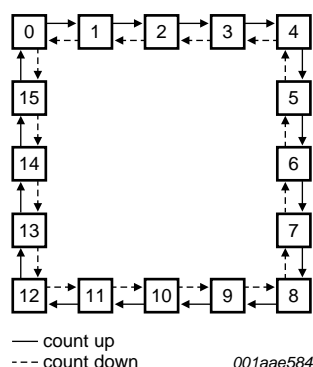


Fig 4. Timing diagram



Logic equations for terminal count:

$$\overline{TCU} = \overline{Q0 \cdot Q1 \cdot Q2 \cdot Q3 \cdot \overline{CPU}}$$

$$\overline{TCD} = \overline{Q0 \cdot Q1 \cdot Q2 \cdot Q3 \cdot \overline{CPD}}$$

Fig 5. State diagram

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+18	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
V <sub>I</sub>	input voltage		-0.5	V <sub>DD</sub> + 0.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
I <sub>I/O</sub>	input/output current		-	±10	mA
I <sub>DD</sub>	supply current		-	50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C
P <sub>tot</sub>	total power dissipation	DIP16 package	[1] -	750	mW
		SO16 package	[2] -	500	mW
P	power dissipation	per output	-	100	mW

[1] For DIP16 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	supply voltage		3	-	15	V
V <sub>I</sub>	input voltage		0	-	V <sub>DD</sub>	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C

Table 5. Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = 25\text{ }^{\circ}\text{C}$		$T_{amb} = 85\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	-	7.5	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	CPU to Qn; see <a href="#">Figure 6</a>	5 V	$183\text{ ns} + (0.55\text{ ns/pF})C_L$	-	210	415	ns
			10 V	$74\text{ ns} + (0.23\text{ ns/pF})C_L$	-	85	165	ns
			15 V	$52\text{ ns} + (0.16\text{ ns/pF})C_L$	-	60	120	ns
	CPD to Qn; see <a href="#">Figure 6</a>		5 V	$183\text{ ns} + (0.55\text{ ns/pF})C_L$	-	210	425	ns
			10 V	$74\text{ ns} + (0.23\text{ ns/pF})C_L$	-	85	170	ns
			15 V	$57\text{ ns} + (0.16\text{ ns/pF})C_L$	-	60	125	ns
	CPU to $\overline{TCU}$ ; see <a href="#">Figure 6</a>		5 V	$98\text{ ns} + (0.55\text{ ns/pF})C_L$	-	125	250	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF})C_L$	-	50	100	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF})C_L$	-	35	70	ns
	CPD to $\overline{TCD}$ ; see <a href="#">Figure 6</a>		5 V	$113\text{ ns} + (0.55\text{ ns/pF})C_L$	-	140	280	ns
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
	MR to Qn; see <a href="#">Figure 6</a>		5 V	$168\text{ ns} + (0.55\text{ ns/pF})C_L$	-	195	390	ns
			10 V	$69\text{ ns} + (0.23\text{ ns/pF})C_L$	-	80	160	ns
			15 V	$52\text{ ns} + (0.16\text{ ns/pF})C_L$	-	60	120	ns
	MR to $\overline{TCD}$		5 V	$338\text{ ns} + (0.55\text{ ns/pF})C_L$	-	365	730	ns
			10 V	$119\text{ ns} + (0.23\text{ ns/pF})C_L$	-	130	265	ns
			15 V	$92\text{ ns} + (0.16\text{ ns/pF})C_L$	-	100	205	ns
	$\overline{PL} \rightarrow Qn$		5 V	$158\text{ ns} + (0.55\text{ ns/pF})C_L$	-	185	360	ns
			10 V	$64\text{ ns} + (0.23\text{ ns/pF})C_L$	-	75	150	ns
			15 V	$47\text{ ns} + (0.16\text{ ns/pF})C_L$	-	55	110	ns



**Table 7. Dynamic characteristics ...continued** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
t <sub>PLH</sub>	LOW to HIGH propagation delay	CPU to Q <sub>n</sub> ; see <a href="#">Figure 6</a>	5 V	143 ns + (0.55 ns/pF)C <sub>L</sub>	-	170	340	ns
			10 V	59 ns + (0.23 ns/pF)C <sub>L</sub>	-	70	140	ns
			15 V	42 ns + (0.16 ns/pF)C <sub>L</sub>	-	50	100	ns
	CPD to Q <sub>n</sub> ; see <a href="#">Figure 6</a>		5 V	143 ns + (0.55 ns/pF)C <sub>L</sub>	-	170	340	ns
			10 V	59 ns + (0.23 ns/pF)C <sub>L</sub>	-	70	140	ns
			15 V	42 ns + (0.16 ns/pF)C <sub>L</sub>	-	50	100	ns
	CPU to $\overline{\text{TCU}}$ ; see <a href="#">Figure 6</a>		5 V	68 ns + (0.55 ns/pF)C <sub>L</sub>	-	95	185	ns
			10 V	29 ns + (0.23 ns/pF)C <sub>L</sub>	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF)C <sub>L</sub>	-	30	60	ns
	CPD to $\overline{\text{TCD}}$ ; see <a href="#">Figure 6</a>		5 V	73 ns + (0.55 ns/pF)C <sub>L</sub>	-	100	195	ns
			10 V	29 ns + (0.23 ns/pF)C <sub>L</sub>	-	40	85	ns
			15 V	22 ns + (0.16 ns/pF)C <sub>L</sub>	-	30	65	ns
	MR to $\overline{\text{TCU}}$		5 V	118 ns + (0.55 ns/pF)C <sub>L</sub>	-	145	285	ns
			10 V	49 ns + (0.23 ns/pF)C <sub>L</sub>	-	60	115	ns
			15 V	37 ns + (0.16 ns/pF)C <sub>L</sub>	-	45	90	ns
	$\overline{\text{PL}}$ to Q <sub>n</sub>		5 V	118 ns + (0.55 ns/pF)C <sub>L</sub>	-	145	290	ns
			10 V	49 ns + (0.23 ns/pF)C <sub>L</sub>	-	60	120	ns
			15 V	37 ns + (0.16 ns/pF)C <sub>L</sub>	-	45	90	ns
t <sub>t</sub>	transition time	see <a href="#">Figure 6</a>	5 V	10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns
f <sub>max</sub>	maximum frequency	see <a href="#">Figure 6</a>	5 V		2.5	5	-	MHz
			10 V		7	14	-	MHz
			15 V		9	18	-	MHz
t <sub>W</sub>	pulse width	CPU or CPD LOW; minimum width; see <a href="#">Figure 6</a>	5 V		150	75	-	ns
			10 V		50	25	-	ns
			15 V		35	20	-	ns
		MR input HIGH; minimum width; see <a href="#">Figure 6</a>	5 V		180	90	-	ns
			10 V		70	35	-	ns
			15 V		60	30	-	ns
		$\overline{\text{PL}}$ input LOW; minimum width; see <a href="#">Figure 6</a>	5 V		120	60	-	ns
			10 V		45	20	-	ns
			15 V		30	15	-	ns
t <sub>rec</sub>	recovery time	MR input; see <a href="#">Figure 6</a>	5 V		125	65	-	ns
			10 V		70	35	-	ns
			15 V		50	25	-	ns
		$\overline{\text{PL}}$ input; see <a href="#">Figure 6</a>	5 V		90	45	-	ns
			10 V		35	15	-	ns
			15 V		25	10	-	ns

**Table 7. Dynamic characteristics ...continued**

$V_{SS} = 0$  V;  $T_{amb} = 25$  °C; for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_{su}$	set-up time	Dn to $\overline{PL}$ ; see <a href="#">Figure 6</a>	5 V		160	80	-	ns
			10 V		60	30	-	ns
			15 V		50	25	-	ns
$t_h$	hold time	Dn to $\overline{PL}$ ; see <a href="#">Figure 6</a>	5 V		+10	-70	-	ns
			10 V		+5	-25	-	ns
			15 V		+5	-20	-	ns

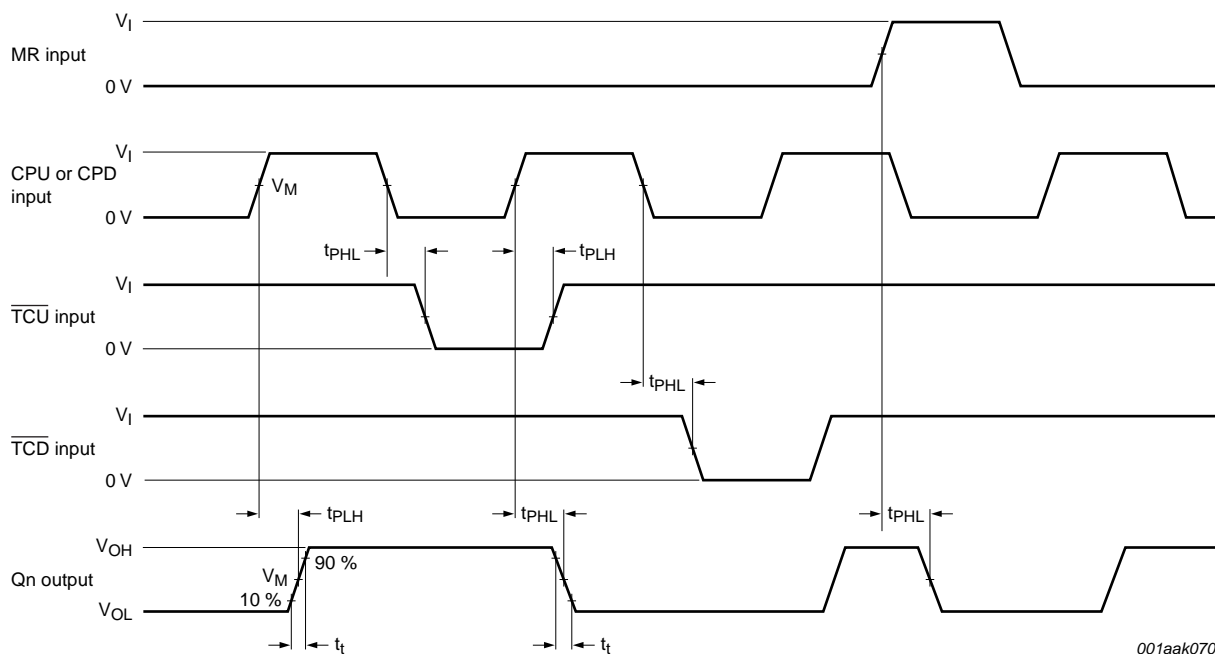
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

**Table 8. Dynamic power dissipation  $P_D$** 

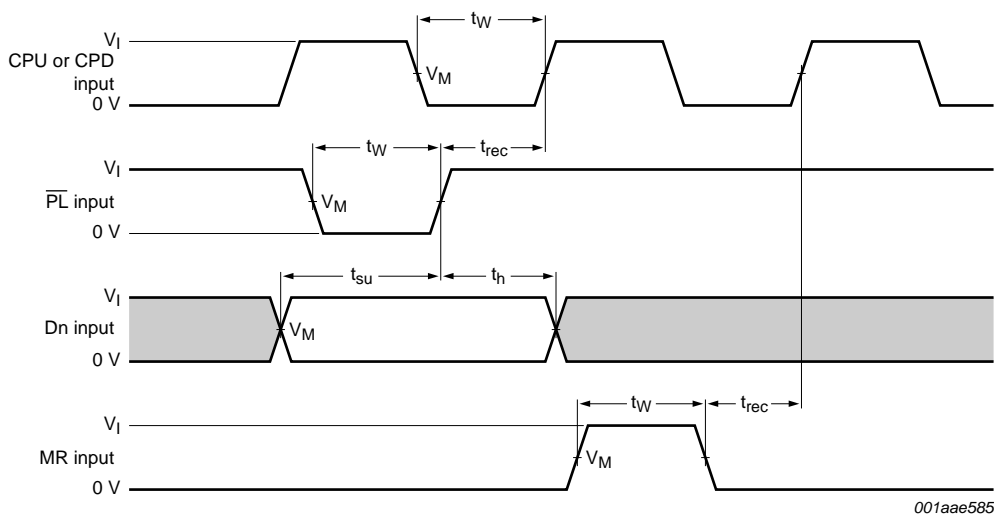
$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0$  V;  $t_r = t_f \leq 20$  ns;  $T_{amb} = 25$  °C.

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu$ W)	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz,
		10 V	$P_D = 2700 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_o$ = output frequency in MHz,
		15 V	$P_D = 7500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.

## 11. Waveforms



a. Propagation delays and output transition times



b.  $\overline{PL}$  and MR recovery times, CPU, CPD,  $\overline{PL}$  and MR minimum pulse widths, and Dn to  $\overline{PL}$  set-up and hold times

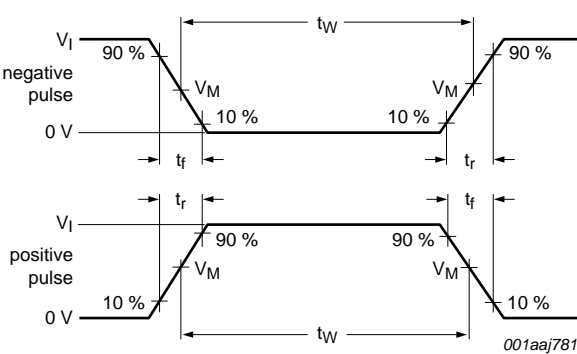
$V_{OH}$  and  $V_{OL}$  are typical output voltage levels that occur with the output load.

Set-up and hold times are shown as positive values but may be specified as negative values.

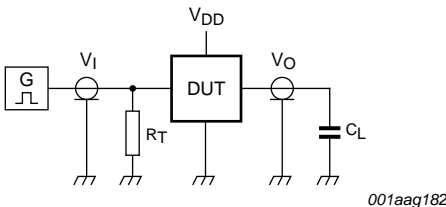
The shaded area is where the data can change for predictable performance.

Measurement points are given in [Table 9](#).

**Fig 6. Waveforms showing switching times**



a. Input waveforms



b. Test circuit

Test data is given in [Table 9](#).

Definitions for test circuit:

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 7. Test circuit for switching times

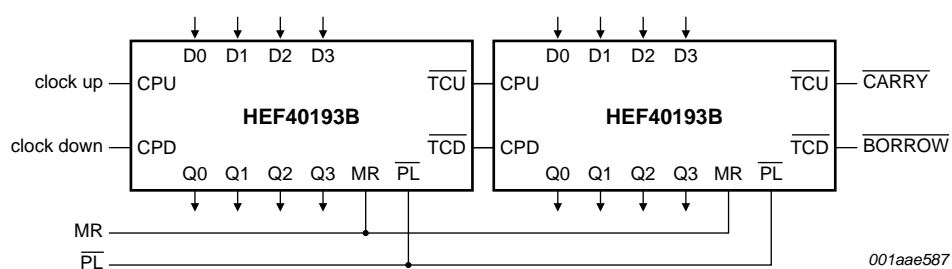
Table 9. Measurement points and test data

Supply voltage	Input			Load
	$V_I$	$V_M$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{DD}$	$0.5V_I$	$\leq 20$ ns	50 pF

## 12. Application information

Some examples of applications for the HEF40193B are:

- Up/down difference counting
- Multistage ripple counting
- Multistage synchronous counting

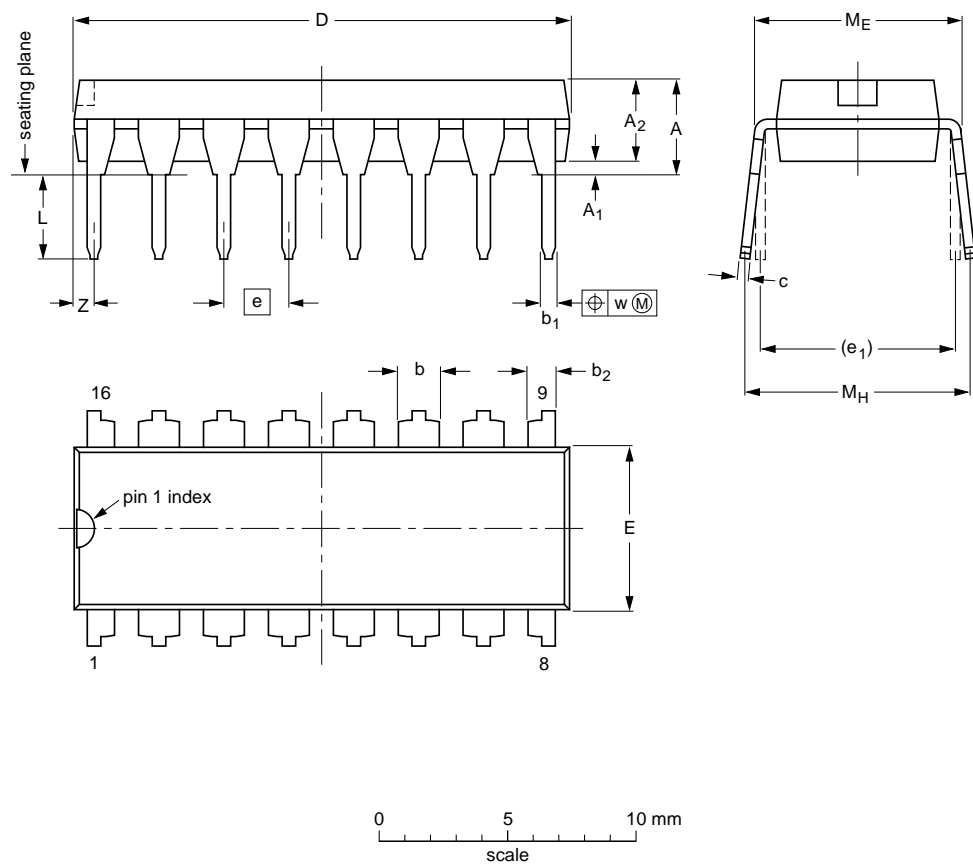


**Fig 8. Example of cascaded HEF40193B ICs**

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)																
UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

**Note**  
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14- 03-02-13

Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

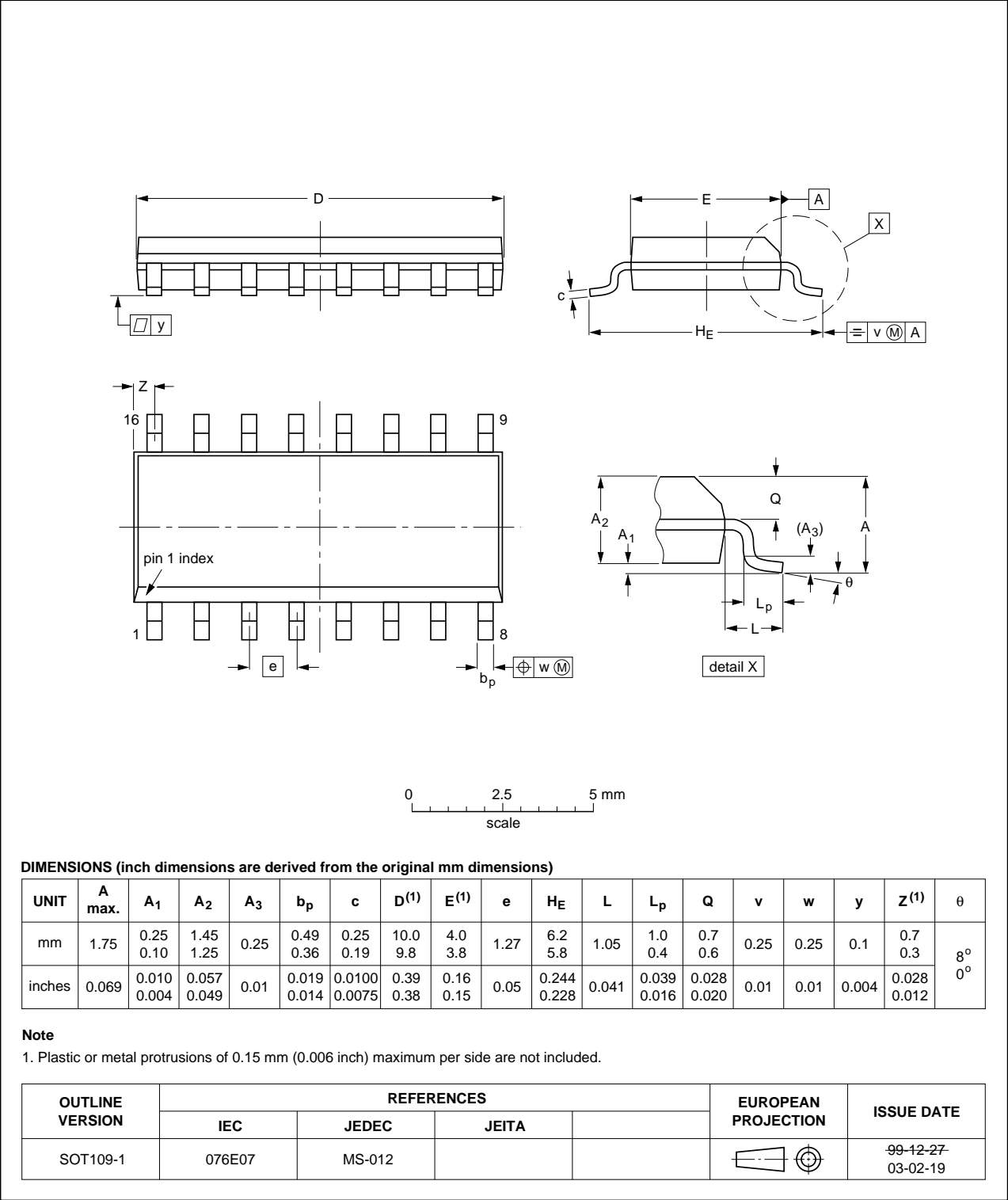


Fig 10. Package outline SOT109-1 (SO16)

## 14. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40193B v.8	20111118	Product data sheet	-	HEF40193B v.7
Modifications:	<ul style="list-style-type: none"><li>• Legal pages updated.</li><li>• Changes in “General description” and “Features and benefits”.</li><li>• Section “Applications” removed.</li></ul>			
HEF40193B v.7	20110914	Product data sheet	-	HEF40193B v.6
HEF40193B v.6	20091222	Product data sheet	-	HEF40193B v.5
HEF40193B v.5	20090615	Product data sheet	-	HEF40193B v.4
HEF40193B v.4	20090505	Product data sheet	-	HEF40193B_CNV v.3
HEF40193B_CNV v.3	19950101	Product specification	-	HEF40193B_CNV v.2
HEF40193B_CNV v.2	19950101	Product specification	-	-



## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 18 November 2011

Document identifier: HEF40193B

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