TVS Diode

Transient Voltage Suppressor Diodes

ESD5V3L1B Series

Bi-directional Low Capacitance ESD / Transient Protection Diode

ESD5V3L1B-02LRH
ESD5V3L1B-02LS

Data Sheet

Revision 1.1, 2012-10-15
Final

Power Management & Multimarket

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Revision History Revision 1, 2011-08-04	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.1, 2012-10-15	
5	**Table 2-1** updated
8/9	**Figure 3-3** and **Figure 3-4** updated

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Last Trademarks Update 2010-10-26

1 Bi-directional Low Capacitance ESD / Transient Protection Diode

1.1 Features

- ESD / transient protection of signal lines in low voltage applications according to:
  - **IEC61000-4-2 (ESD): ±20 kV (air / contact)**
  - **IEC61000-4-4 (EFT): 40 A (5/50 ns)**
- Bi-directional, symmetrical working voltage up to V_{RWM} = ±5.3 V
- Low capacitance: C_L **= 5 pF** (typical)
- Low clamping voltage, low dynamic resistance down to: R_{DYN} = 0.23 Ω (typical)
- Pb-free (RoHS compliant) and halogen free package, very small form factor: 0.62 x 0.32 x 0.31 mm^3

RoHS

1.2 Application Examples

- Keypad, touchpad, buttons, convenience keys
- LCD displays, Camera, audio lines, mobile communication, Consumer products (E-Book, MP3, DVD, DSC...)
- Notebooks tablets and desktop computers and their peripherals

1.3 Product Description

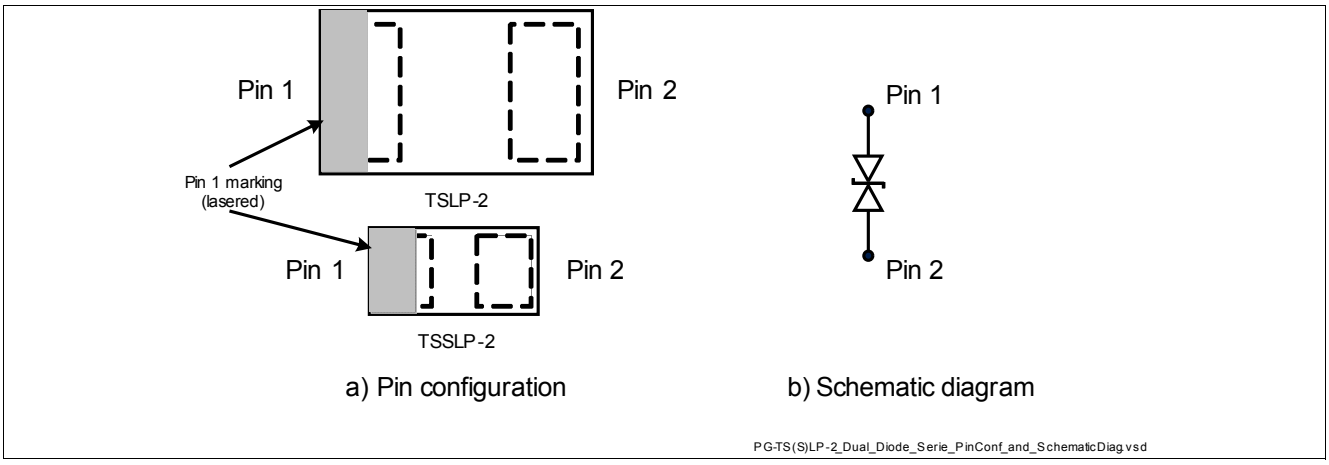

Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Ordering Information

Type	Package	Configuration	Marking code
ESD5V3L1B-02LRH	PG-TSLP-2-17	1 line, bi-directional	4
ESD5V3L1B-02LS	PG-TSSLP-2-1	1 line, bi-directional	C

2 Characteristics

Table 2-1 Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD contact discharge[1)]	V_{ESD}	–	–	20	kV
Peak pulse current (t_p = 8/20 µs)[2)]	I_{PP}	–	3	2.5	A
Peak pulse power (t_p = 8/20 µs)[2)]	P_{PP}	–	39	30	W
Operating temperature range	T_{OP}	-40	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2

2) I_{PP} according IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

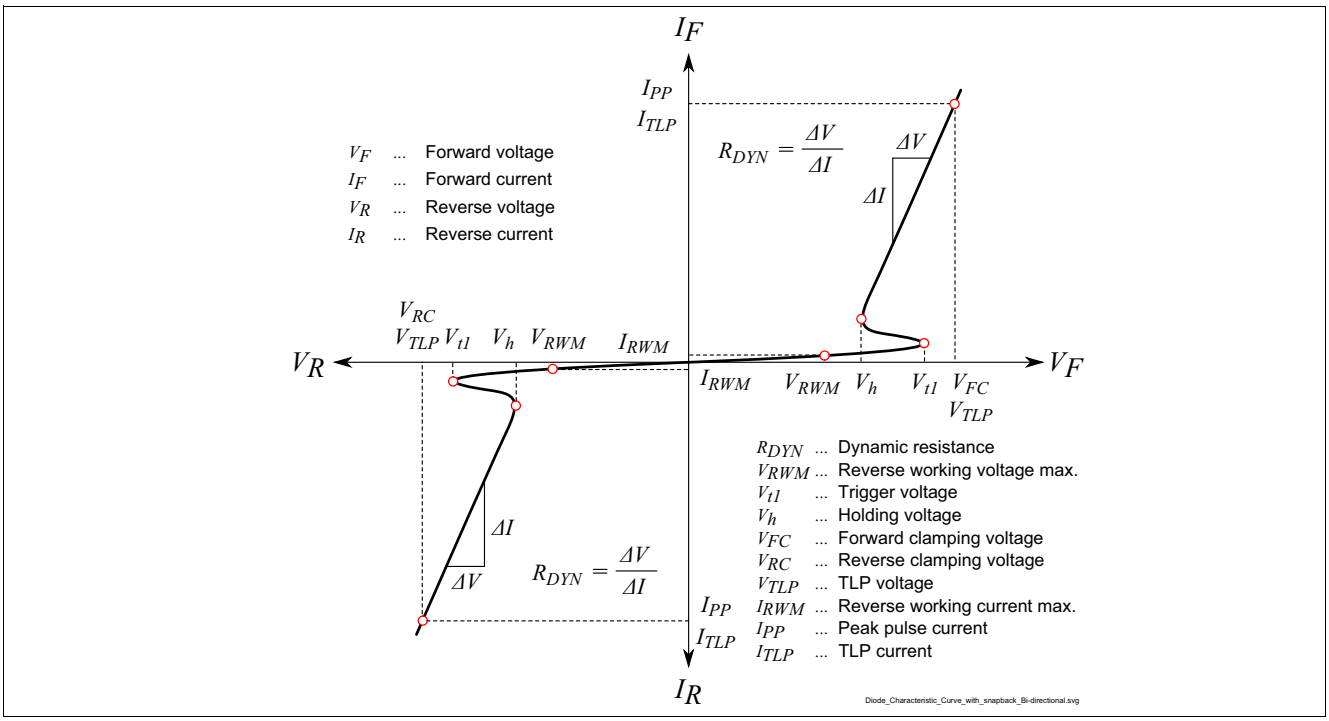

Figure 2-1 Definitions of electrical characteristics

Table 2-2 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-5.3	–	5.3	V	
Breakdown voltage	V_{BR}	6	–	10	V	I_{BR} = 1 mA
Reverse current	I_R	–	–	100	nA	V_R = 5.3 V

Table 2-3 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	4	–	7	pF	V_R = 0 V, f = 1 MHz
Series inductance	L_S	–	0.4	–	nH	PG-TSLP-2-17
		–	0.2	–		PG-TSSLP-2-1

Table 2-4 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[1)]	V_{CL}	–	10.2	–	V	I_{TLP} = 16 A, from Pin 1 to Pin 2
		–	13.2	–		I_{TLP} = 30 A, from Pin 1 to Pin 2
		–	12.1	–		I_{TLP} = 16 A, from Pin 2 to Pin 1
		–	17.2	–		I_{TLP} = 30 A, from Pin 2 to Pin 1
Clamping voltage[2)]		–	8.5	–		I_{PP} = 1 A, from Pin 1 to Pin 2
		–	9.8	–		I_{PP} = 2.5 A, from Pin 1 to Pin 2
		–	8.5	–		I_{PP} = 1 A, from Pin 2 to Pin 1
		–	10.4	–		I_{PP} = 2.5 A, from Pin 2 to Pin 1
Dynamic resistance[2)]	R_{DYN}	–	0.22	–	Ω	Pin 1 to Pin 2
		–	0.37	–	Ω	Pin 2 to Pin 1

1) Please refer to Application Note AN210 [1]. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 300ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristics between I_{PP1} = 10 A and I_{PP2} = 40 A.

2) I_{PP} according to IEC61000-4-5 (t_p = 8/20 µs)

3 Typical Characteristics at T_A = 25 °C, unless otherwise specified

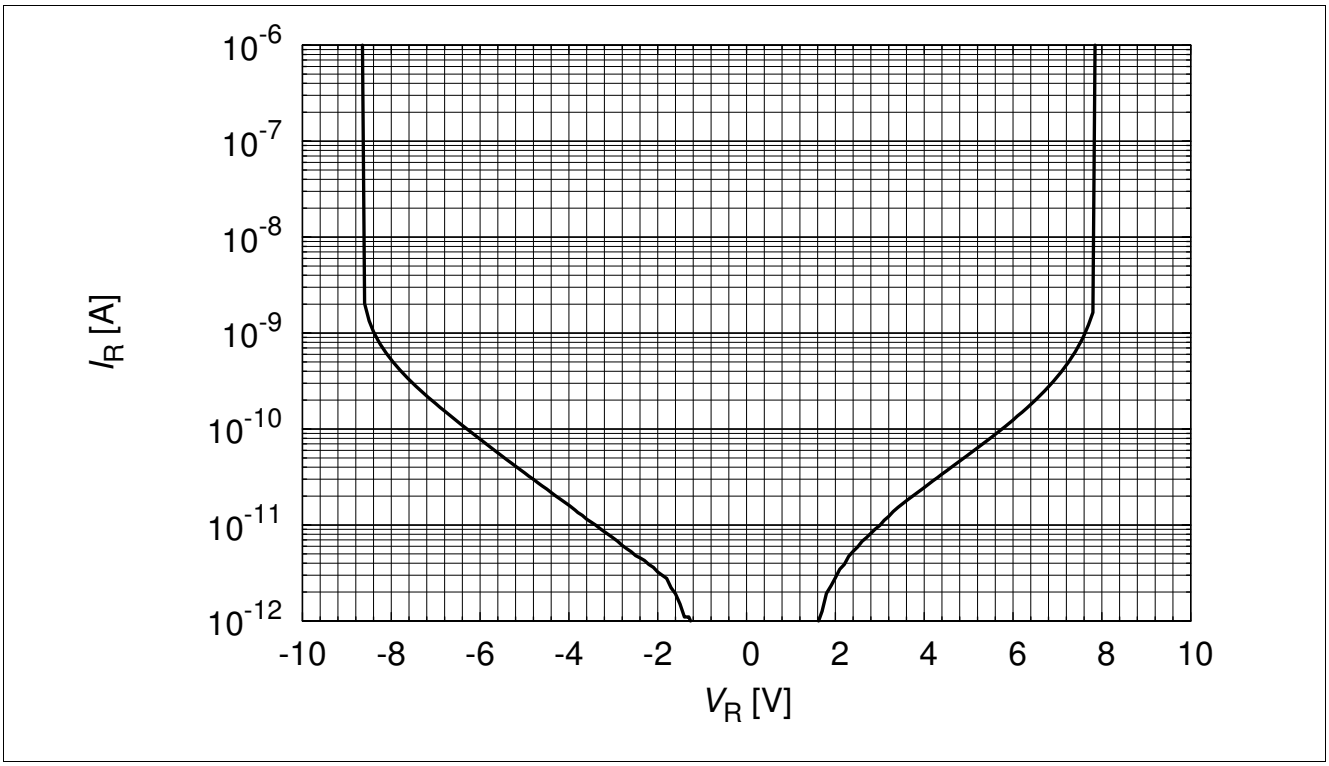

Figure 3-1 Reverse current: $I_R = f(V_R)$

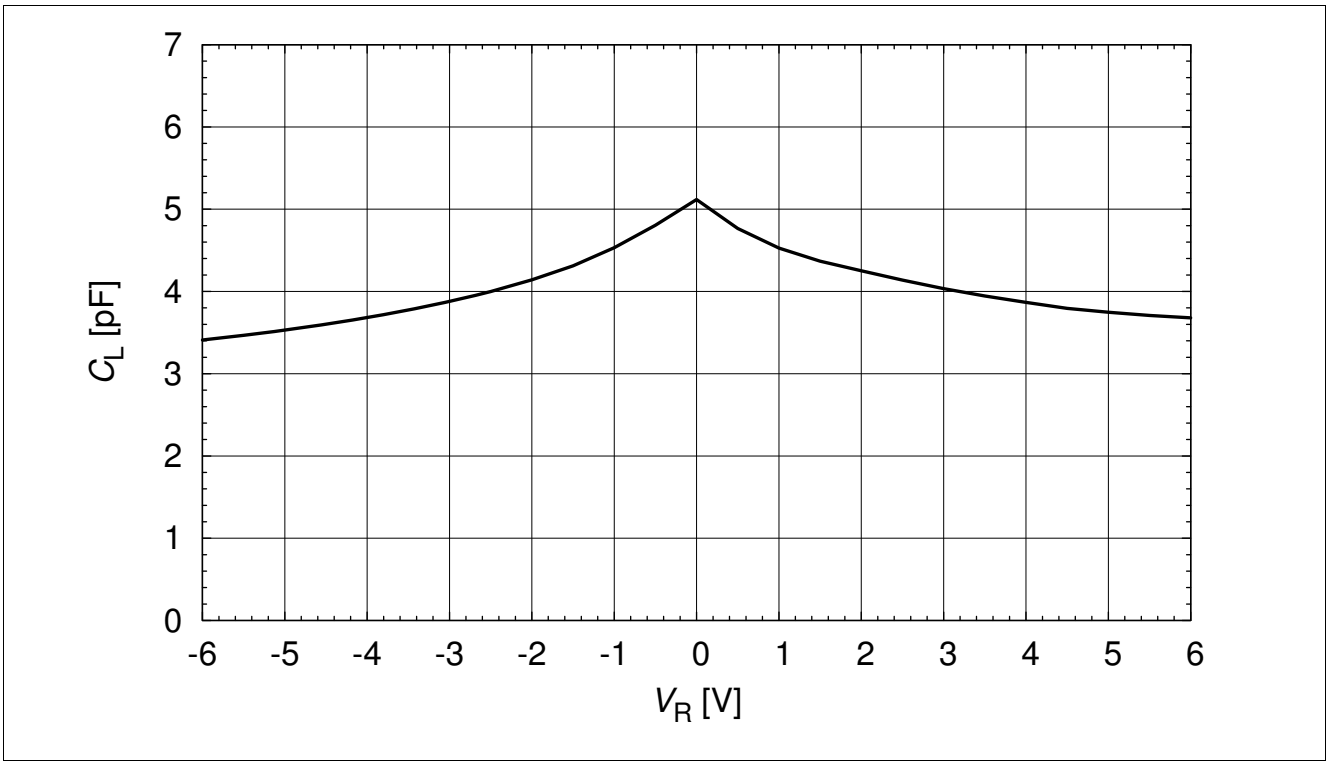

Figure 3-2 Line capacitance: $C_L = f(V_R)$, f = 1MHz

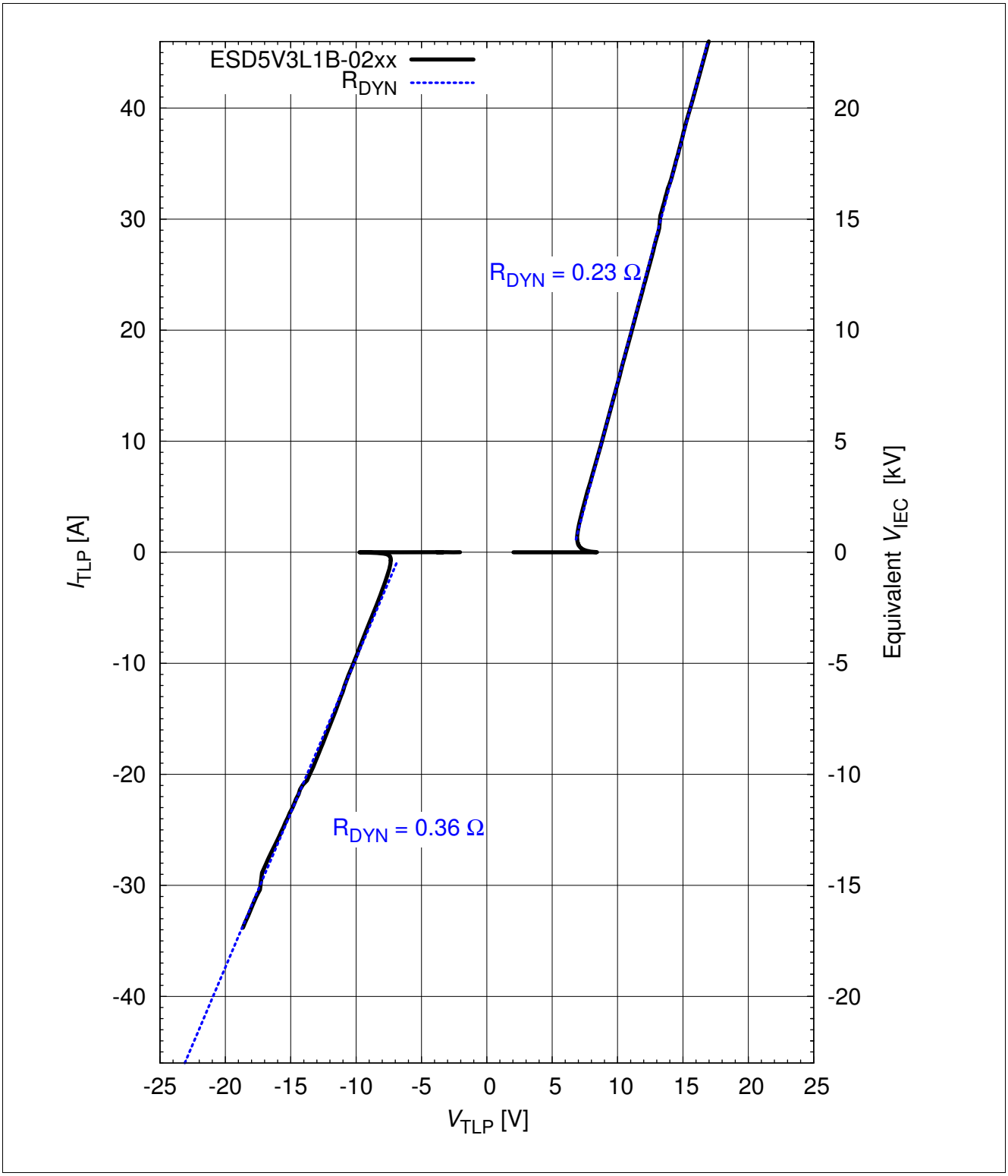

Figure 3-3 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} averaging window: t_1 = ns to t_2 = 60 ns, extraction of dynamic resistance using squares fit to TLP characteristics between I_{TLP1} = 10 A and I_{TLP2} = 40 mA. Please refer to Application Note AN210[1]

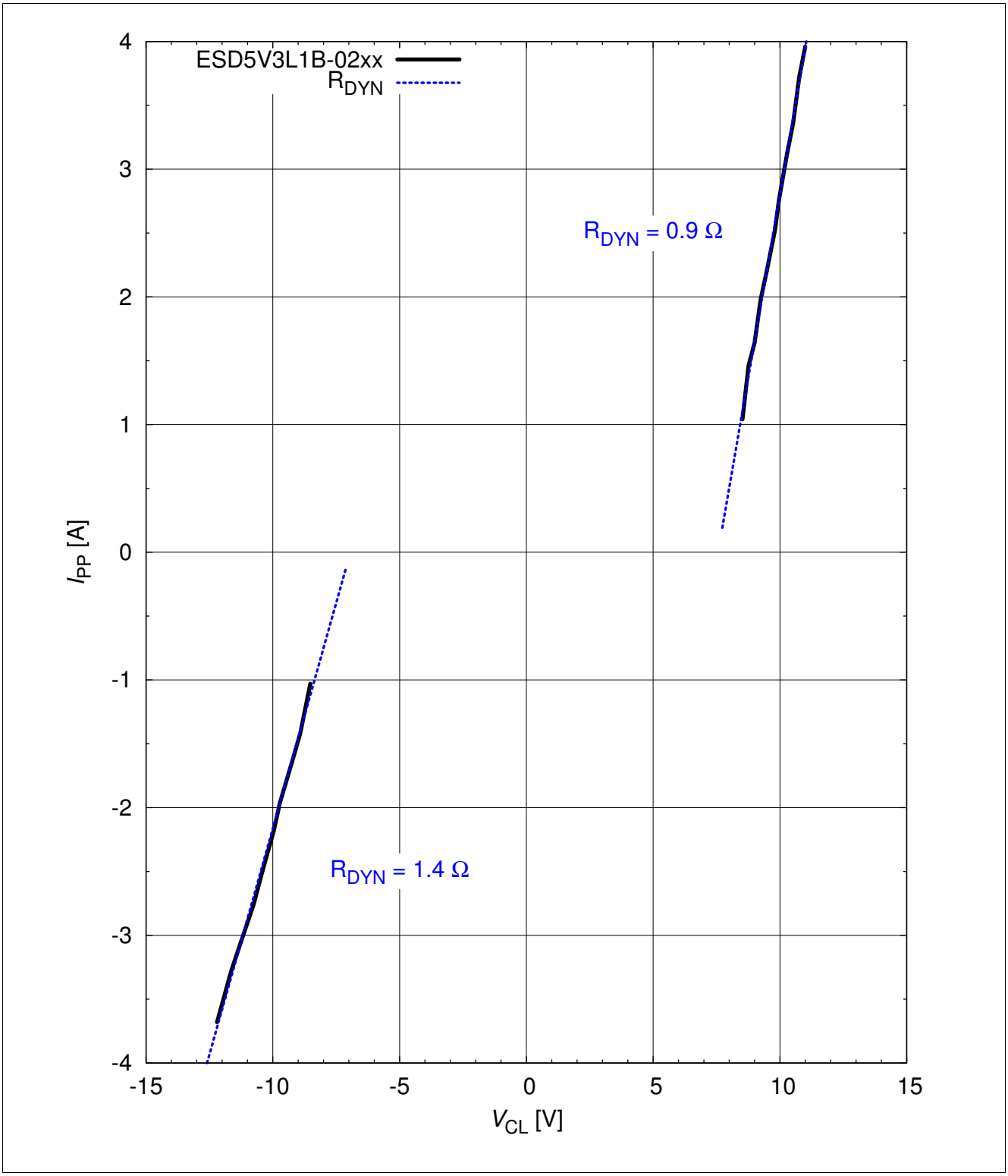

Figure 3-4 Pulse current (IEC61000-4-5) versus clamping voltage: $I_{PP} = f(V_{CL})$

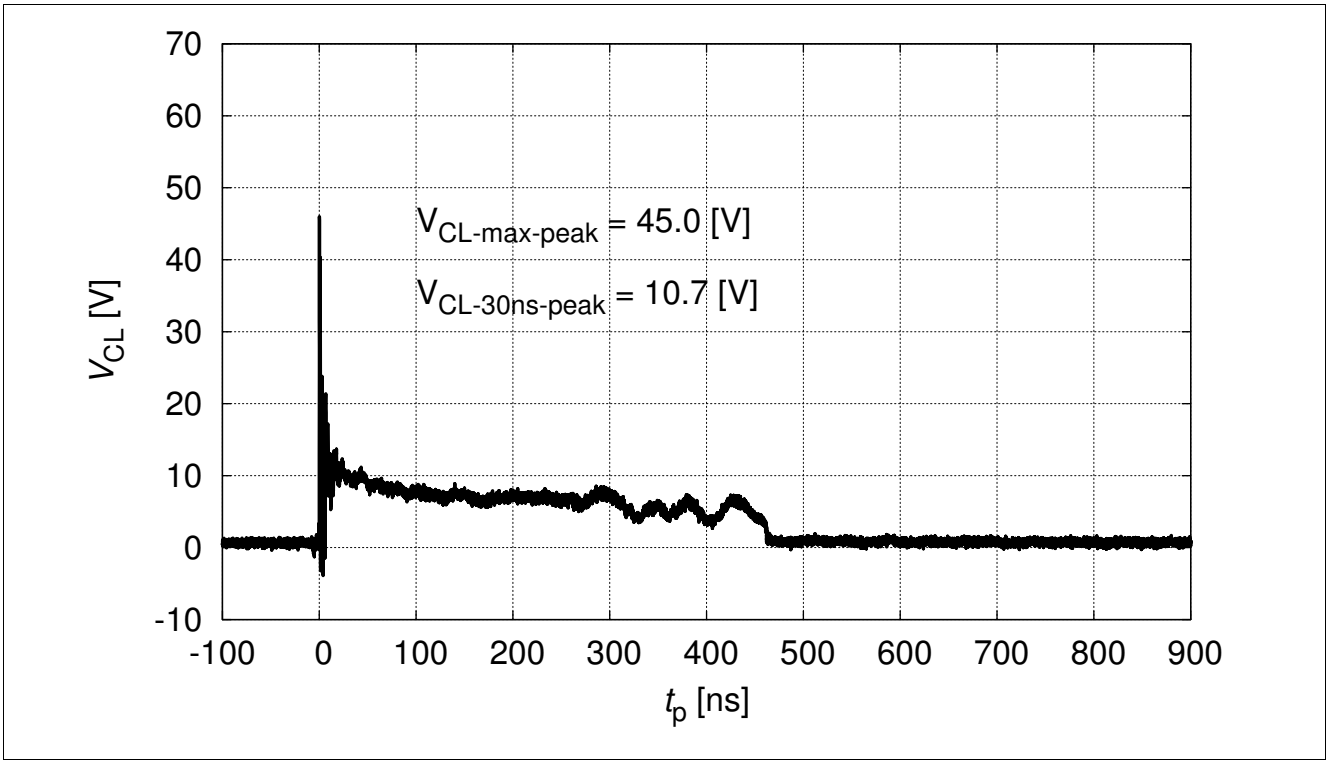

Figure 3-5 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

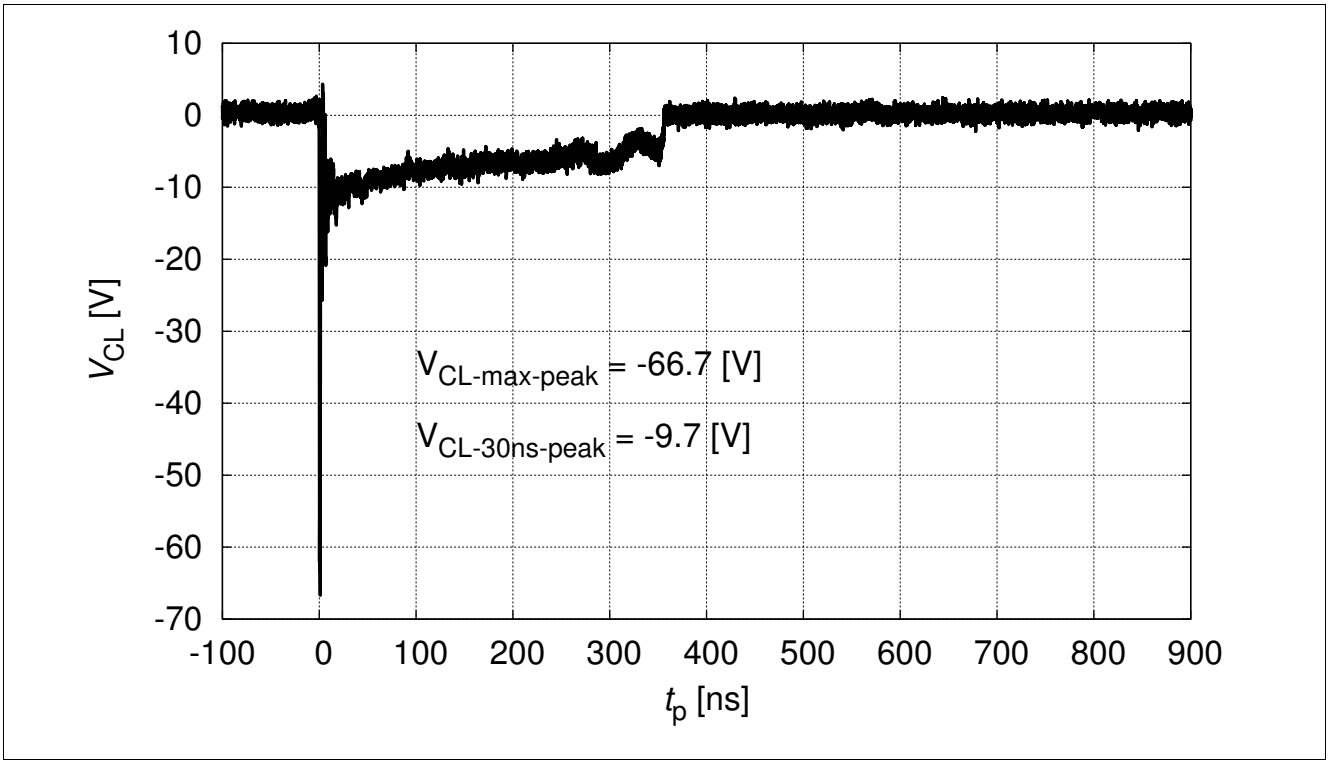

Figure 3-6 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2

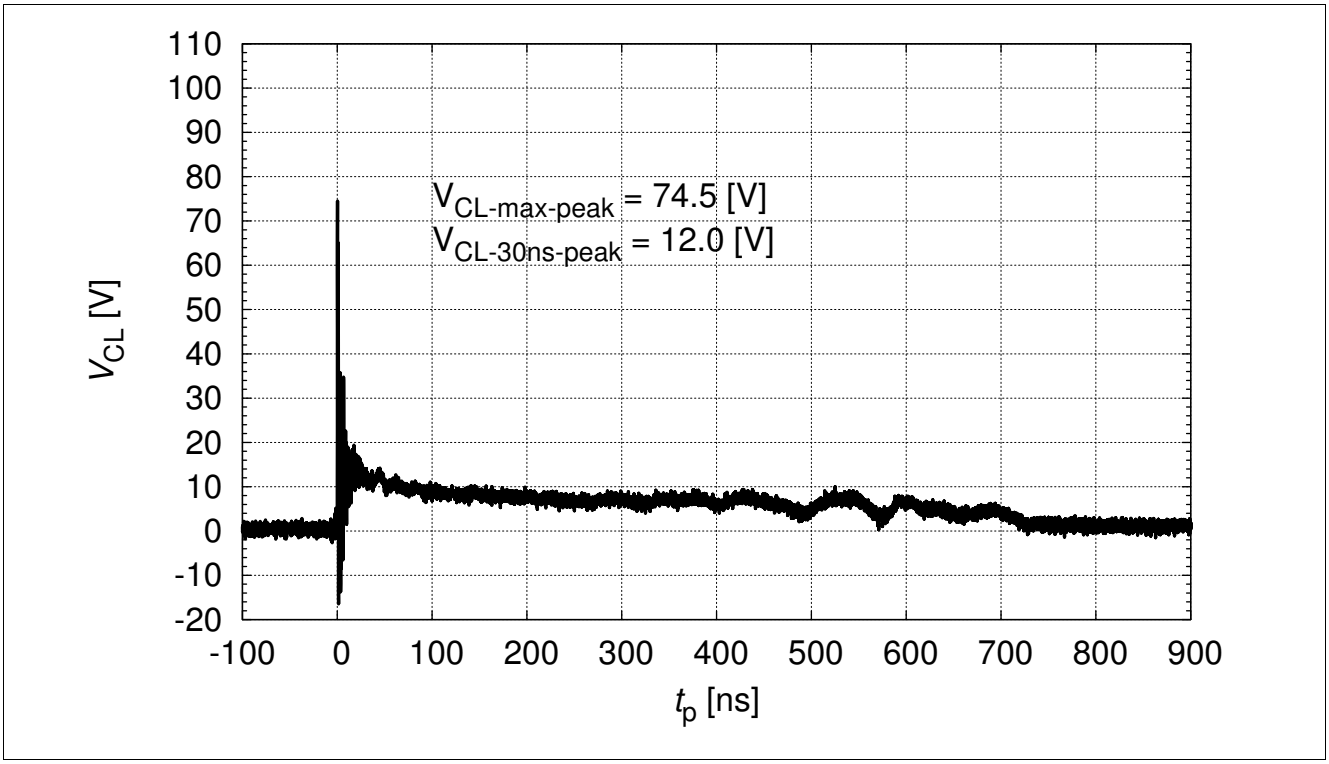

Figure 3-7 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

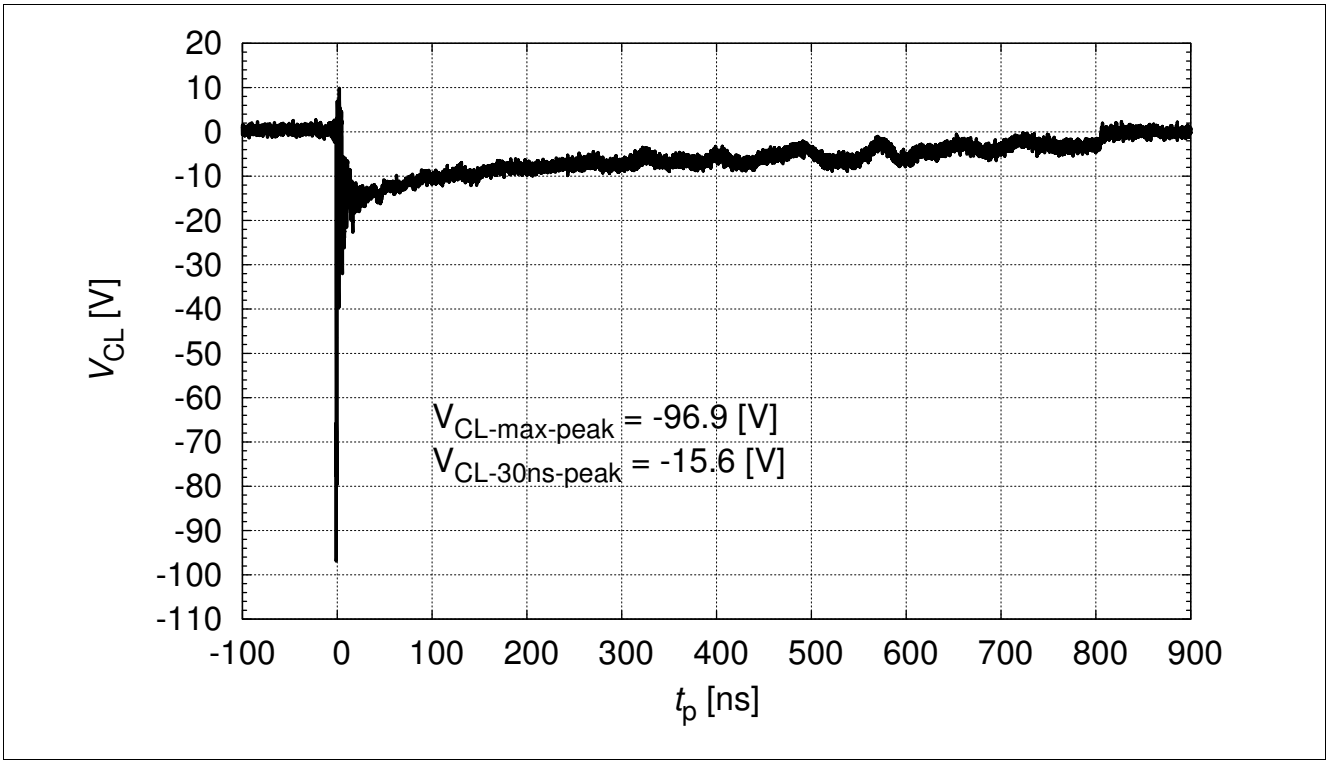

Figure 3-8 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2

4 Application Information

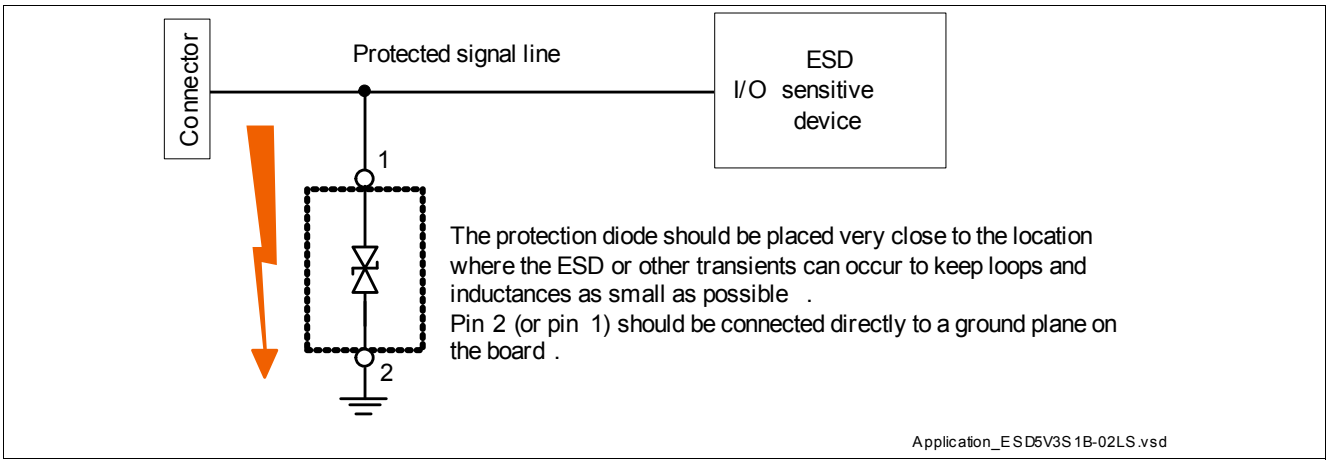

Figure 4-1 Single line, bi-directional ESD / Transient protection

5 Ordering Information Scheme (Examples)

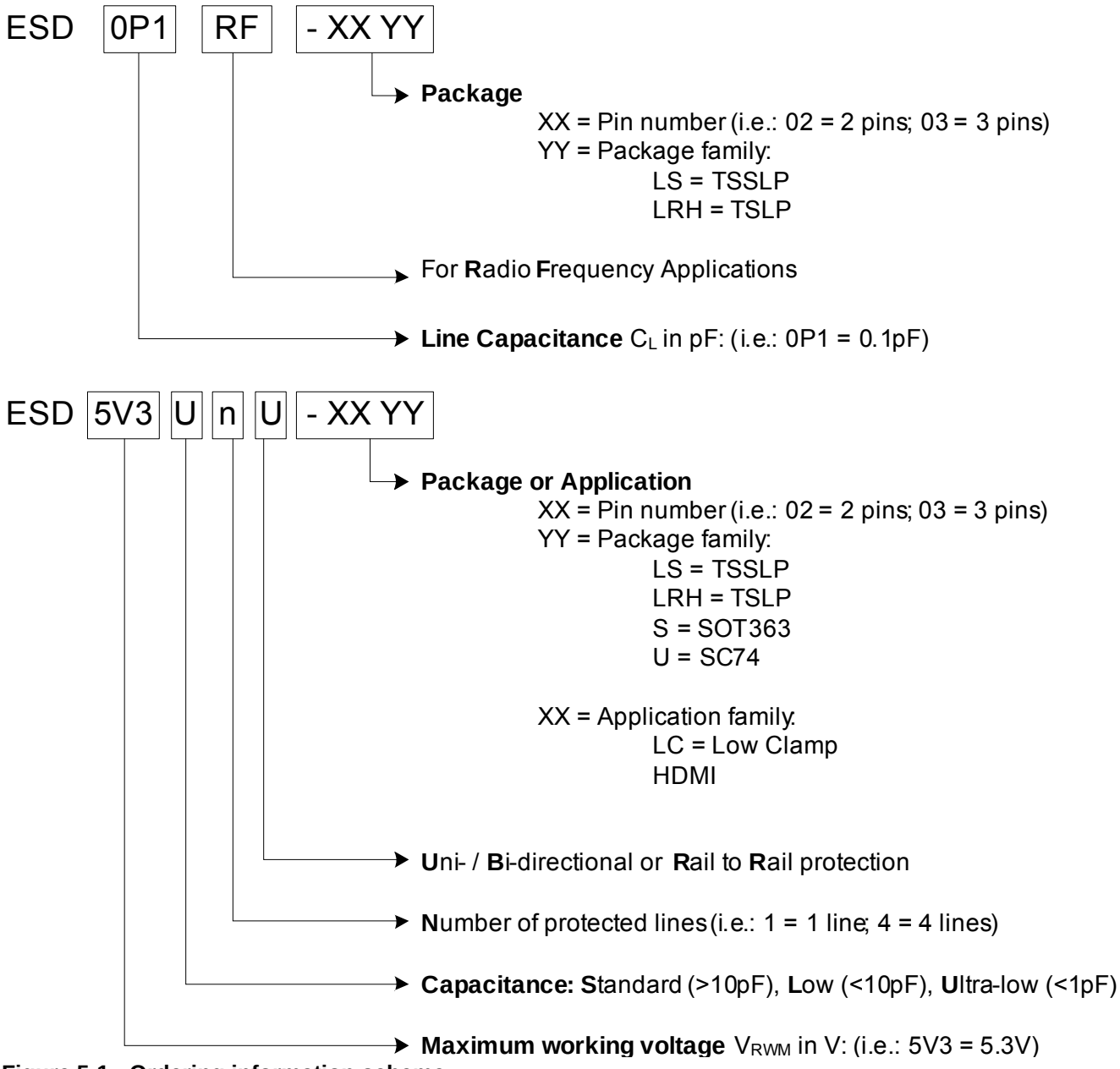

Figure 5-1 Ordering information scheme

6 Package Information

6.1 PG-TSLP-2-17 (mm) [2]

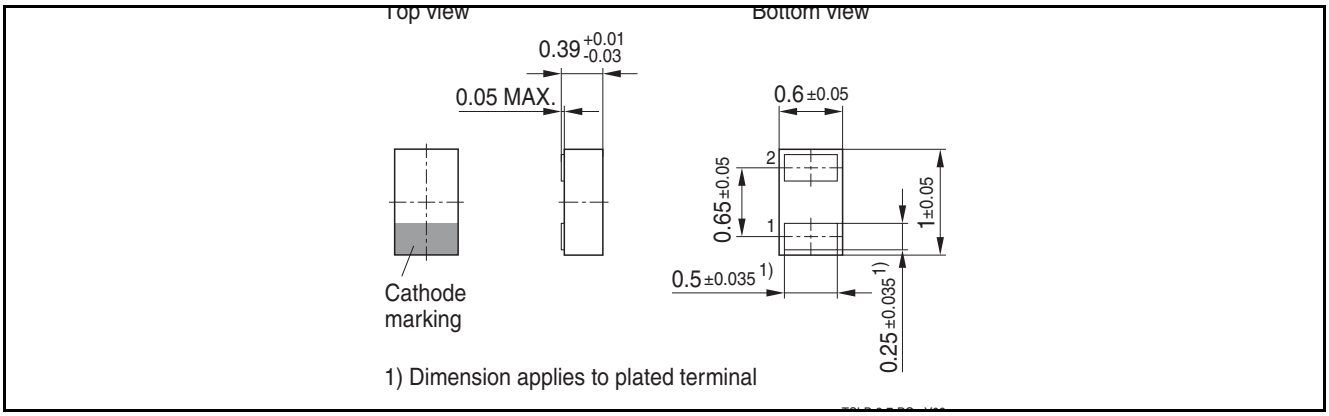

Figure 6-1 PG-TSLP-2-17: Package overview

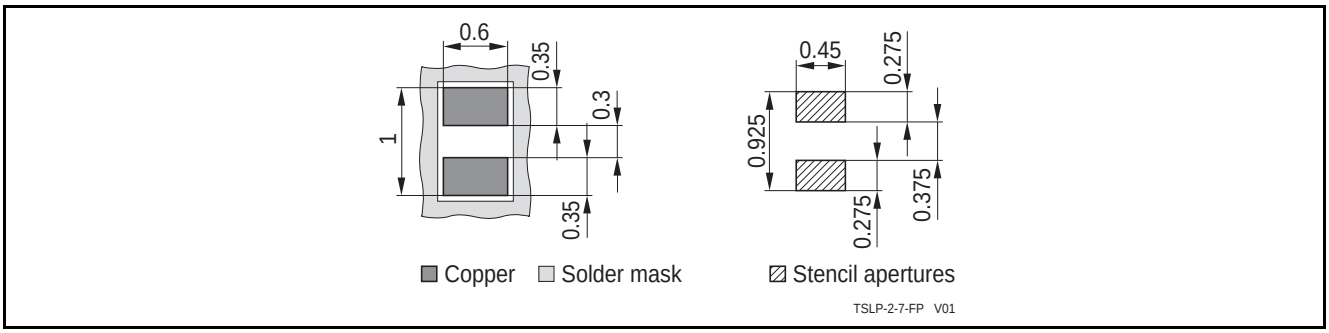

Figure 6-2 PG-TSLP-2-17: Footprint

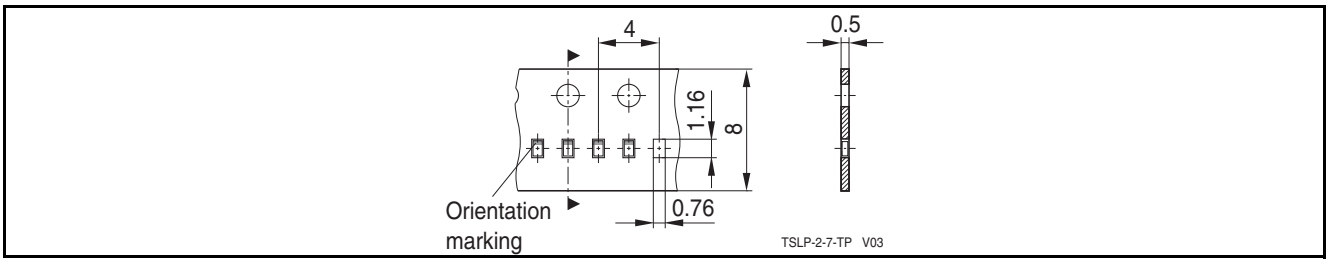

Figure 6-3 PG-TSLP-2-17: Packing

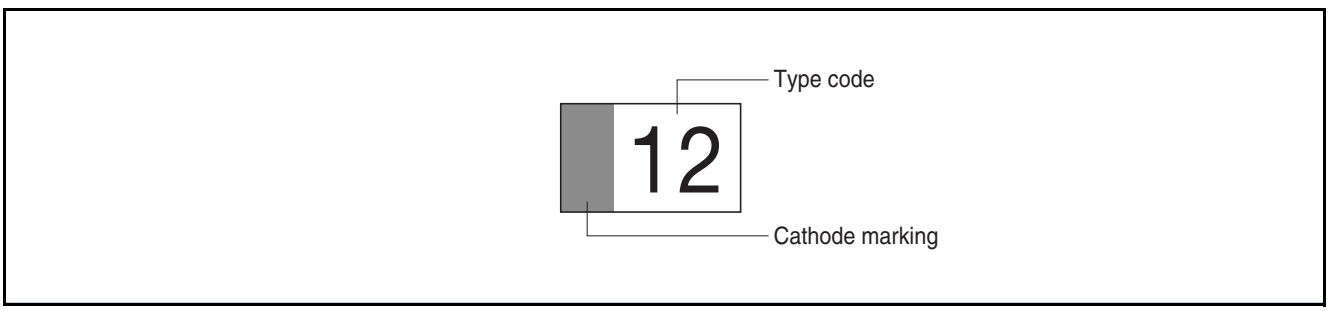

Figure 6-4 PG-TSLP-2-17: Marking (example)

6.2 PG-TSSLP-2-1 (mm) [2]

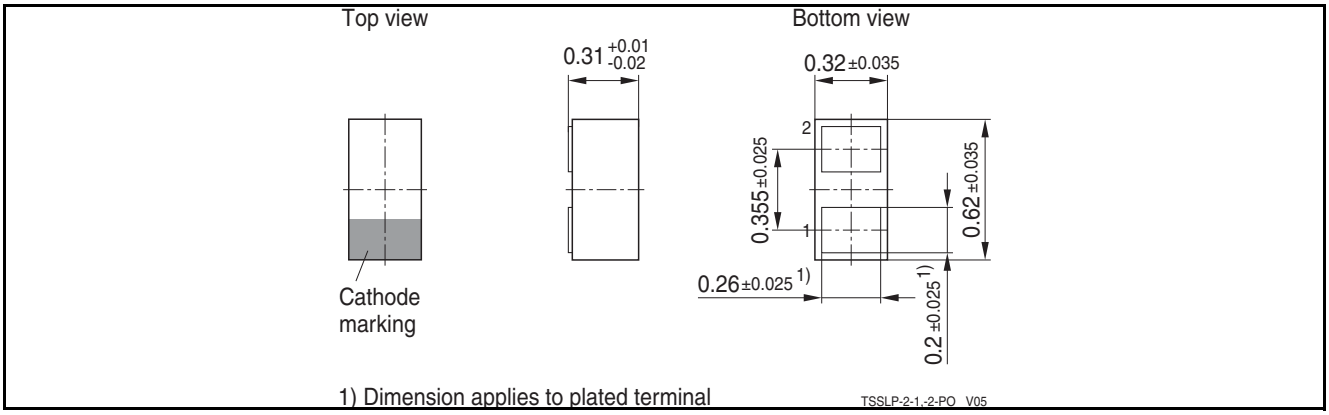

Figure 6-5 PG-TSSLP-2-1: Package overview

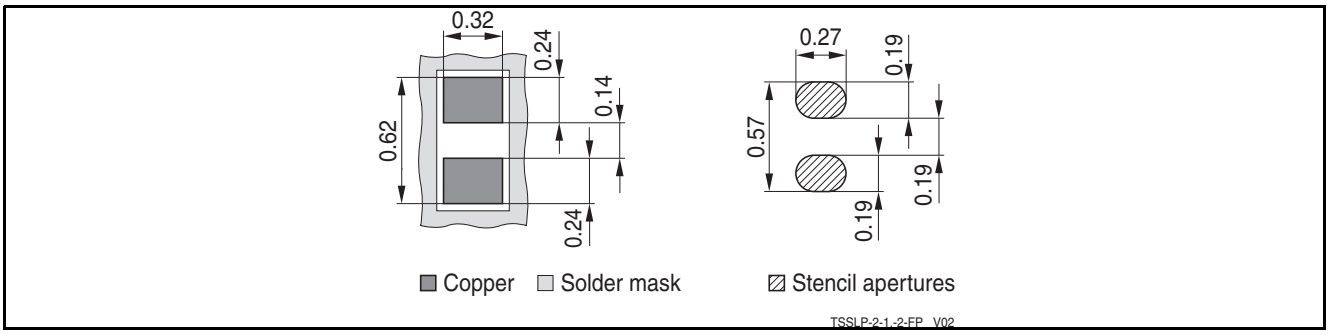

Figure 6-6 PG-TSSLP-2-1: Footprint

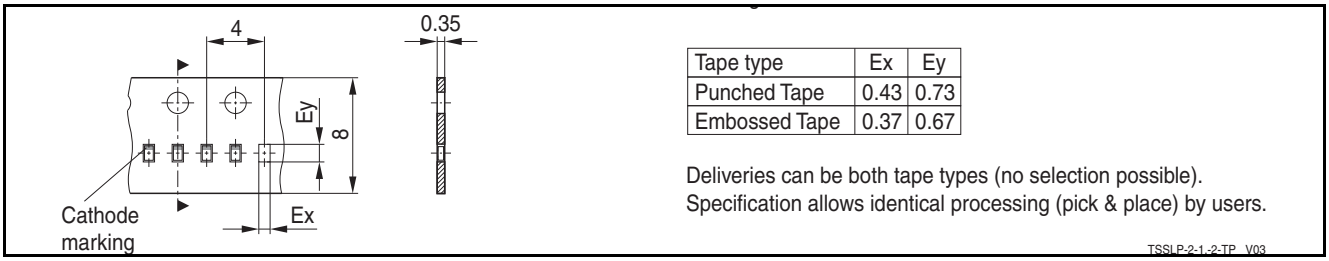

Figure 6-7 PG-TSSLP-2-1: Packing

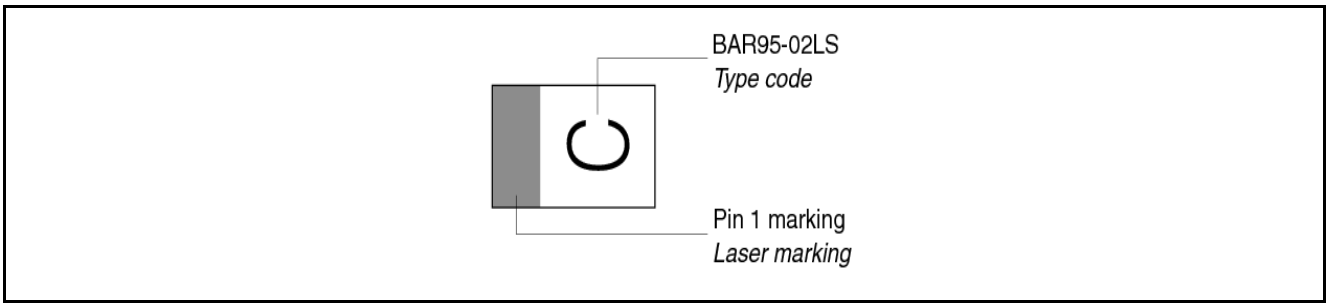

Figure 6-8 PG-TSSLP-2-1: Marking (example)

References

[1] Infineon AG - **Application Note AN210:** Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

[2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

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